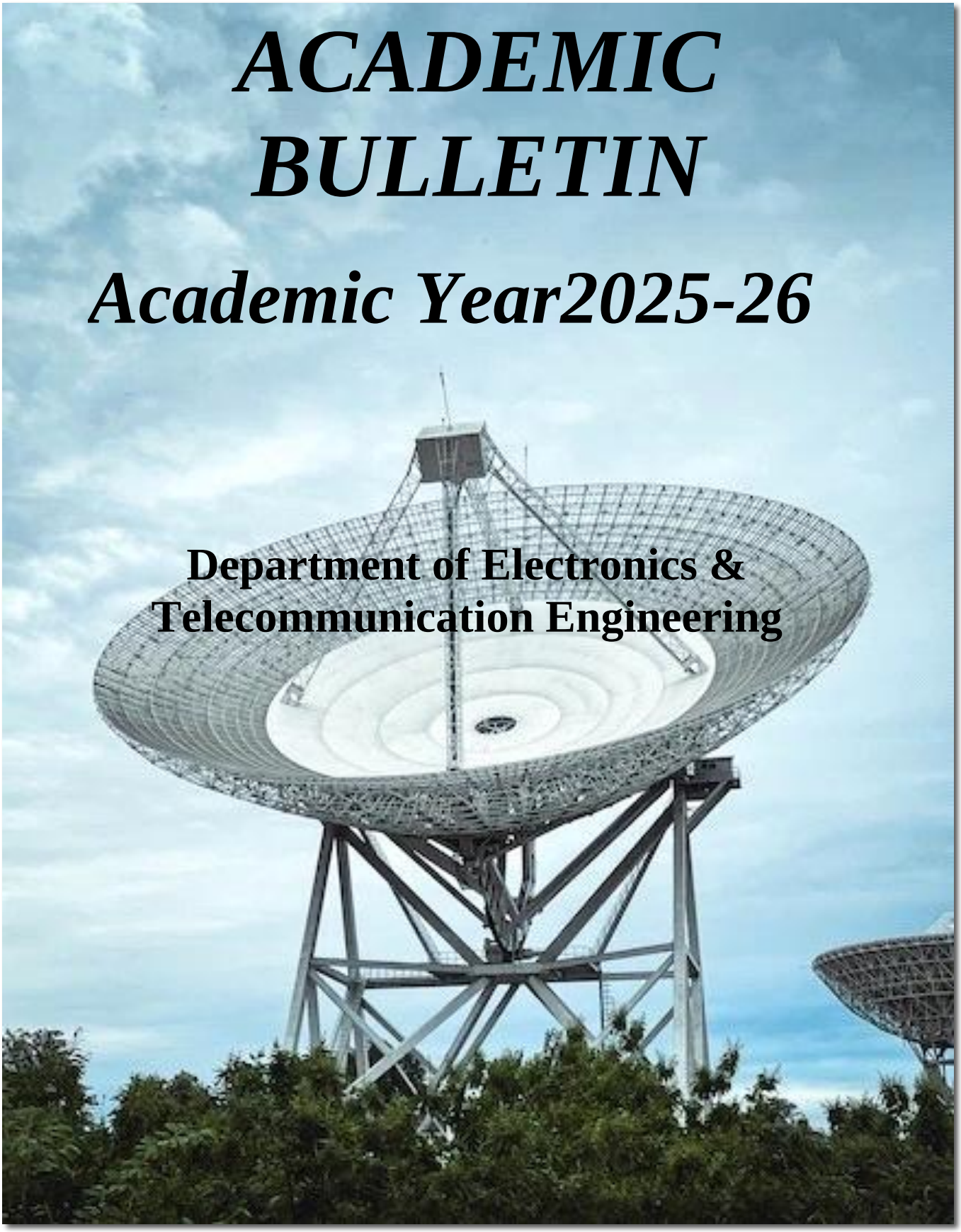
Shri Vile Parle Kelavani Mandal's
DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING
(Autonomous College Affiliated to the University of Mumbai)
NAAC Accredited with "A" Grade (CGPA : 3.18)

ACADEMIC BULLETIN

Academic Year2025-26



Department of Electronics & Telecommunication Engineering

Shri Vile Parle Kelavani Mandal's
DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING
(Autonomous College Affiliated to the University of Mumbai)
NAAC Accredited with "A" Grade (CGPA : 3.18)

ACADEMIC BULLETIN

July 2025- June 2026

Department of Electronics & Telecommunication Engineering

Prepared by:

Dr. Supriya Dicholkar
(Assistant Professor, EXTC, DJSCE)

Prof. Amit A. Deshmukh
(Professor & Head EXTC, DJSCE)

ACADEMIC BULLETIN

Period: 1st July 2025 – 31st December 2025

Department of Electronics and Telecommunication

1. ABOUT DEPARTMENT

1.1 Department Information

- Started in the year 1999 with the intake of 30 and which was increased to 60 in the subsequentyear.
- The intake was increased to 120 in the Academic Year 2010 – 11.
- In the Academic Year 2011 – 12, Department has started M.E. Program in Electronics & telecommunication with an intake of 18 students.
- For the first time Department got NBA accreditation for two years from January 2013. In second Outcome based evaluation, Department got NBA accreditation for three years from July 2017.
- The Department started with Ph.D. program in Academic Year 2015 – 16 with an intake of 10 students.
- The department is having highly qualified, experienced and dedicated faculties and supportingstaff.
- Well-equipped labs and fully air-conditioned classrooms with projectors.
- The intake was increased to 180 in the Academic Year 2022 – 23.

1.2 Vision of the Department

To develop technically competent and socially responsible Electronics and Telecommunication engineers capable of fulfilling expectations at indigenous and global levels.

1.3 Mission of the Department

- To provide a conducive educational environment for students by providing goodinfrastructural facilities, knowledge base and excellent faculty support.
- To provide a strong foundation of core knowledge and exposure to research culture.
- To motivate learners to acquire adequate professional and soft skills, to develop personalitytraits and eventually transform them as life-long learners.
- To strive and achieve practical exposure by maintaining good rapport with industry and professional network.

1.4 Program Educational Objectives (PEOs)

- **PEO1:** To prepare learners for graduate studies by providing strong foundation of basic sciences, computer programing and thus, develop analytical aptitude, and problem-solving abilities.
- **PEO2:** To develop a fundamental understanding of electronic & integrated circuits, communication systems and allied disciplines.
- **PEO3:** To develop core competency and expertise in the diverse areas of communication covering Signal processing, Electromagnetic Engineering, Embedded Systems, ComputerCommunication and Advanced Wireless Networks domains.
- **PEO4:** To inculcate competencies and aptitude in extending acquired technical knowledge to solve real life issues with high professional and ethical standards.
- **PEO5:** To develop proficiency in soft skills and deliver adequate personality traits to enablethe pass outs to pursue higher education, to find competitive employment opportunities and/or pursue entrepreneurial ventures.

1.5 Program Specific Outcomes (PSOs)

- Design and implement electronic systems that perform analog and digital signal processing functions as applied in embedded systems, multimedia processing and VLSI design.
- Design and implement necessary components (circuits, antennas, microwave devices) of modern RF/Wired/Wireless communication systems.
- Cultivate necessary soft skills, aptitude and programming skills to solve real-world problems.

2. ADMINISTRATION

IETE COMMITTEE

Prof. Amit Deshmukh — Dr. Anuja Odhekar

PROJECT COORDINATOR

Prof. Amit Deshmukh — Dr. Ameya Kadam

DEPARTMENTAL LIBRARY

Prof. Amit Deshmukh — Prof. Archana Chaudhari

ALUMNI COMMITTEE

Prof. Amit Deshmukh — Prof. Ranjushree Pal

NBA CORE COMMITTEE

Prof. Amit Deshmukh — Dr. V. V. Kelkar (PC)

Dr. Ameya Kadam (PC)

AUTONOMY COMMITTEE

Dr. Poonam Kadam — Prof. Shreeja Nair

TIME-TABLE COMMITTEE

Prof. Archana Chaudhary — Prof. Mrunalini Pimpale

Prof. Tushar Sawant

PLACEMENT COORDINATOR

Dr. Aarti Ambekar — Dr. Supriya Dicholkar

Prof. Tushar Sawant

NPTEL and IBM COORDINATOR

Dr. V. V. Kelkar

3. IETE- SF

The Electronics and Telecommunication Department of Dwarkadas. J. Sanghvi College of Engineering presents Institution of Electronics and Telecommunication Engineers- Student Forum (IETE-SF). The student chapter with a working force committee of 22, consisting of second year and third year students, hosted a few of the most quintessential and technically challenging events. A membership drive was conducted at the start of the year with an overwhelming response. (www.djsceietesf.com)

IETE Organizing Committee Structure

IETE SF Branch Counsellor: - Dr. Anuja Odhekar

Chairman	Anmol Parekh
Vice-Chairperson	Krish Tawde
Secretary	Jiya Mevada
Treasurer	Ahaan Deshpande
DJ-Strike Coordinator	Om Kulkarni Payal Vaishnav

Head Of Departments:	
Publicity	Rudra Nisar Advait Sawant
Marketing	Krishna Misra Tanvi Mehta
Technical	Shubham Tayade Abbas Damaniya
Infotech	Aditya Ralhan Agrim Tawani
Creatives	Jyotiraditya Bhat
Events	Aryan Bhalkar, Prayag Kartha
Editorial	Akanshka Raina, Garima Singh
Book Bank	Om Kulkarni
Component Bank	Om Kulkarni

4. DEPARTMENT ACTIVITIES

4.1 Value Added Program under IETE-SF

Book Bank

IETE-SF provides the students with a book bank facility where they can issue reference books at nominal rates for the entire semester. Students who want a better insight into the subject avail this facility as these reference books aid in developing a good understanding of the topics and enable them to consolidate their foundation of the subject. Book bank has more than 60 book titles as per the syllabus requirement for 3rd to 8th semester. This activity not only motivates students to use reference books prescribed in syllabus but also explore them in the library management system. The alumni who worked as "Book-Bank" coordinators received paid assistance-ship in the library during their master program.

Component Bank

IETE-SF provides a component bank facility where students can borrow electronic components which they require for executing multiple projects both in and outside of the curriculum. They can utilize the facility by initially paying 50% of the cost and getting a refund of 20% on returning the components, provided that they are undamaged.

Department of Electronics and Telecommunication

4.2 FDP on Copyright Registration Filling

- Date- 23rd August 2025
- Venue- RF Lab, 5th floor, DJSCE
- Time- 11:30 am- 01:30 pm

OBJECTIVE:

The seminar was organized to:

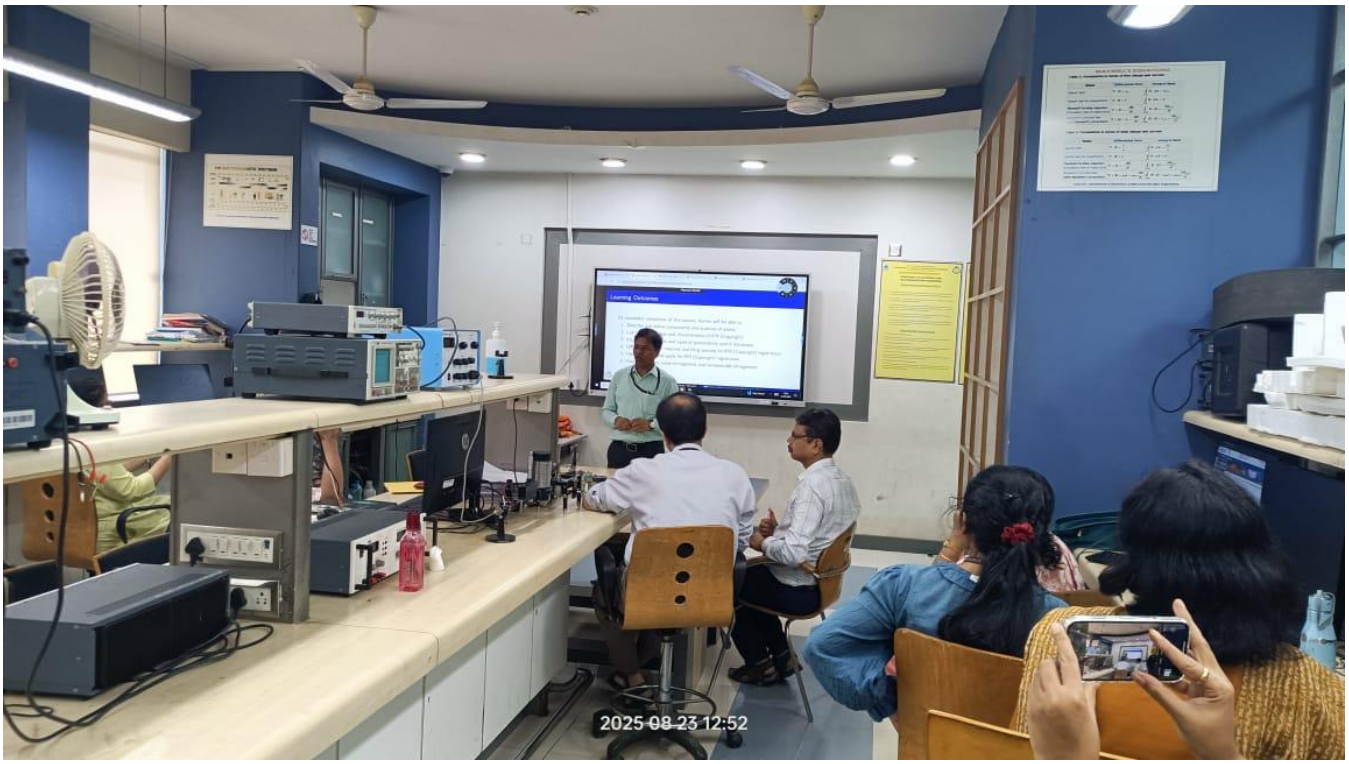
- Discuss and define types and importance of IPR to know who benefits and how.
- Elaborate infringement and elaborate precautions and remedies.
- Provide participants with skills to draft and file the IP (Copyright)

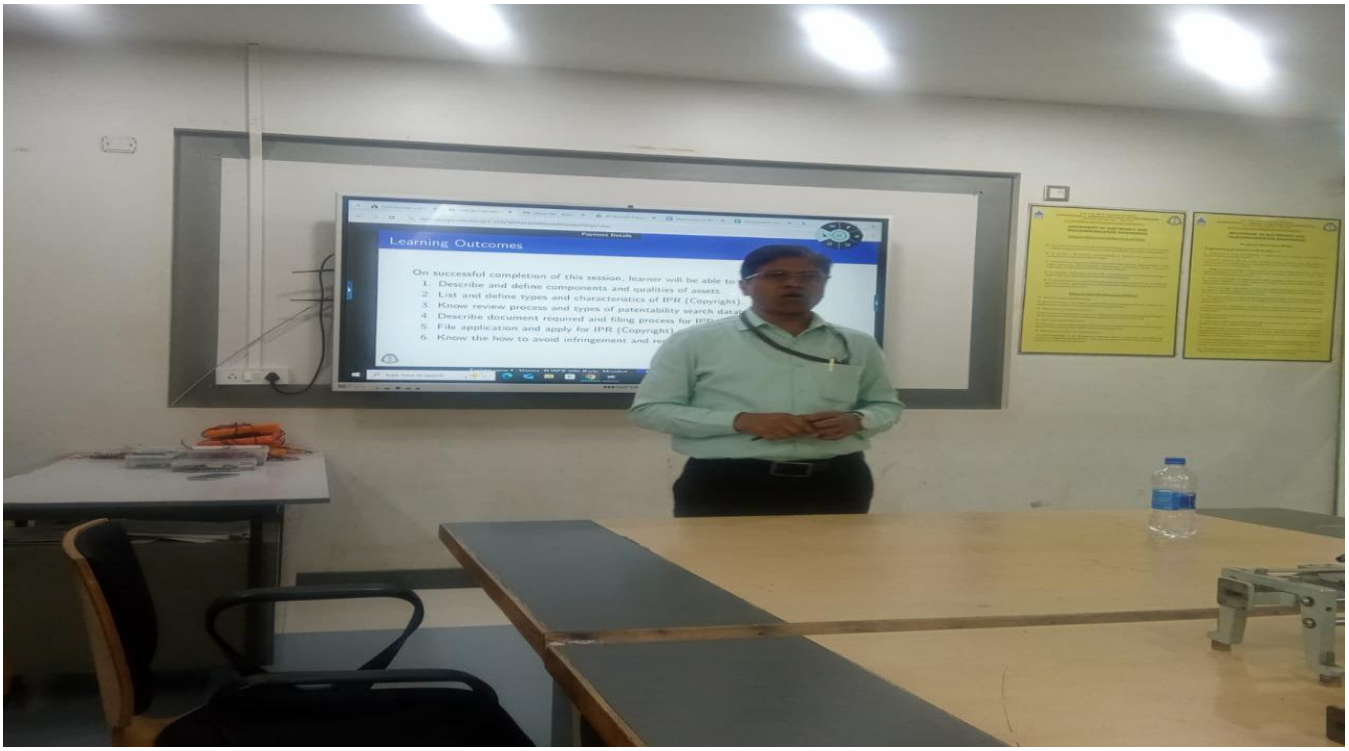
CONTENT:

The Copyright Registration Filling seminar was organized for EXTC faculties to familiarize with Online Filing of Copyright Registration Form and Intellectual Property Rights: Meaning, Types, Importance of it. The aim of the seminar was to provide a clear understanding of the Classify and define different types of assets, discuss and define types and importance of IPR to know who benefits and how, show structure and describe the filing process to register IPRs (Copyright), elaborate infringement and elaborate precautions and remedies, develop within the participant ability to formulate and register IP (Copyright) and provide participants with skills to draft and file the IP (Copyright). search, selection, and organization of relevant research work. Participants learned the techniques for crafting a solid patent application in a multifaceted endeavour which demands attention to detail, strategic foresight, and expert guidance. Key consideration can maximize future success for innovations patentability. Copyrights not only protects invention but also way for commercialization/collaboration. IP registration is an opportunity to value our inventions; It is motivation for continued innovation and collaboration.

Pictures:

Department of Electronics and Telecommunication





Department of Electronics and Telecommunication

4.3 Online Seminar on How to Write Review Paper: Step by Step Guide

- Date- 13th September 2025
- Venue- Online through MS teams
- Time- 11:30 am- 01:30 pm

OBJECTIVE:

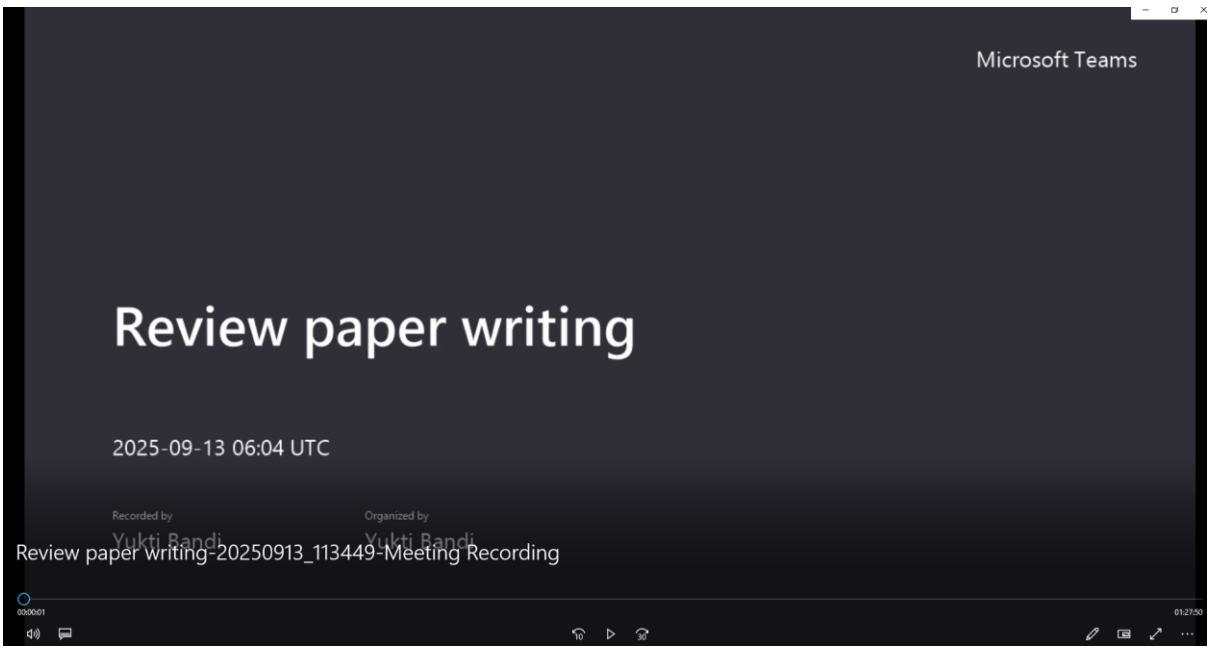
The seminar was organized to:

- Understand the concept and importance of review papers in research.
- Explore systematic methods for searching, selecting, and organizing literature**.**
- Learn proper structuring, citation, and referencing of review articles

CONTENT:

The Review Paper Writing Seminar was organized to familiarize SY and TY B. Tech participants with the purpose and significance of review articles in academic research. The aim of the seminar was to provide a clear understanding of the structure and essential components of a high-quality review paper. It focussed on developing skills for systematic literature search, selection, and organization of relevant research work. Participants learned the techniques for critical analysis, comparison, and synthesis of existing studies. The seminar also emphasized ethical research practices, proper citation, and plagiarism avoidance.

Pictures:



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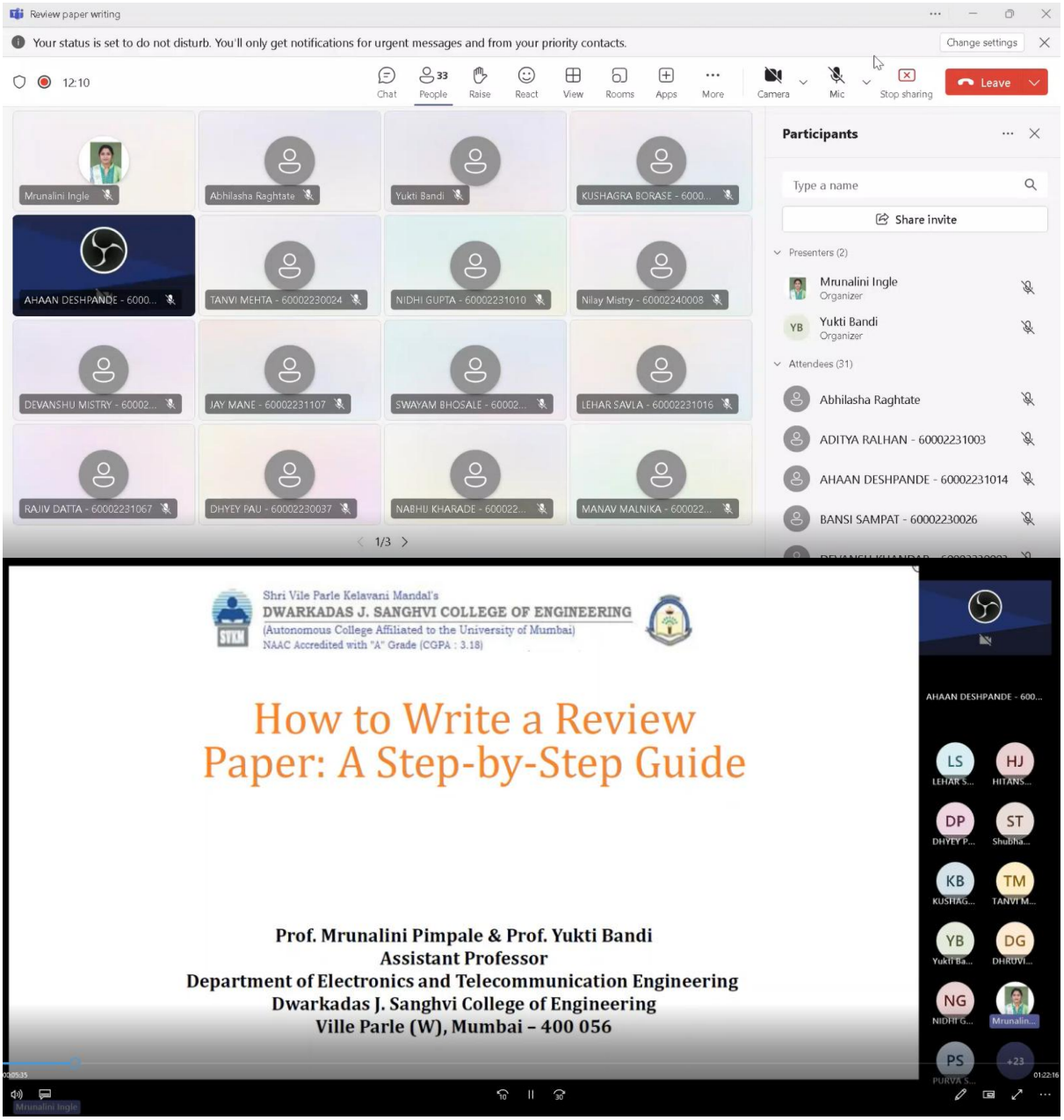


Department of Electronics and Telecommunication

4.4 Industry Interaction On Drone Pilot Training under IETE-SF

- Date- 9th October 2025
- Venue- EXTC Department 5th floor
- Time- 12:30 p.m. - 3:30 p.m.

OBJECTIVE:

- A deeper understanding of drone design principles, pilot training protocols, aviation safety norms, and the wide spectrum of real-world applications that are transforming industries today.
- Bridge the gap between academic learning and industry practice, showing us how technology quite literally takes flight when innovation meets discipline.
- Deepened technical understanding and curiosity to explore this exciting field further

CONTENT:

On 9th October, 2025 on behalf of the IETE Students' Forum and the Department of Electronics and Telecommunication Engineering (EXTC) Department of Dwarkadas J. Sanghvi College of Engineering (DJSCE) organized an Industry Interaction on Drone Pilot Training. The event aimed to achieve deeper understanding of drone design principles, pilot training protocols, aviation safety norms, and the wide spectrum of real-world applications that are transforming industries today with the guidance of two distinguished experts — Mr. Nandkishor Kadu and Dr. Bhaurao Badak, both DGCA-Certified Remote Pilot Instructors. Mr. Kadu and Dr. Badal are affiliated to very first RPTO in Vidharbha region, out of the 13 in Maharashtra.

EVENT PROCEEDINGS:

The event began with felicitating Mr. Nandkishor Kadu and Dr. Bhaurao Badak. This was an interactive session where the students got to learn about the world of UAVs (Unmanned Aerial Vehicles) — commonly known as drones. Mr. Kadu and Dr Badal both explained the importance of drones in National Security and Indian government regulations. How the different parts of drones like sensors, motors, batteries and communication work and function together? They also spoke about different types of drones, such as fixed-wing, rotary-wing, and hybrid models, and explained how they fly using concepts like Bernoulli's principle.

Indian government rules and DGCA regulations, including flying zones (red, yellow, green), licensing, and type certification was also spoken by the speaker. They also learned how quad copters move using throttle, pitch, roll, and yaw to control their flight smoothly. The speakers shared how drones are now being used in so many areas like farming, construction, oil and gas inspections, mapping, and even in disaster relief operations. They also talked about the different tools or "payloads" drones can carry, such as cameras, LiDAR sensors, or even fire extinguishers for emergencies.

The session was wrapped up by discussing the future of Drone Technology, AI powered drones, solar powered drones that can be in air for longer, military uses, swarm of drones working together, etc. The

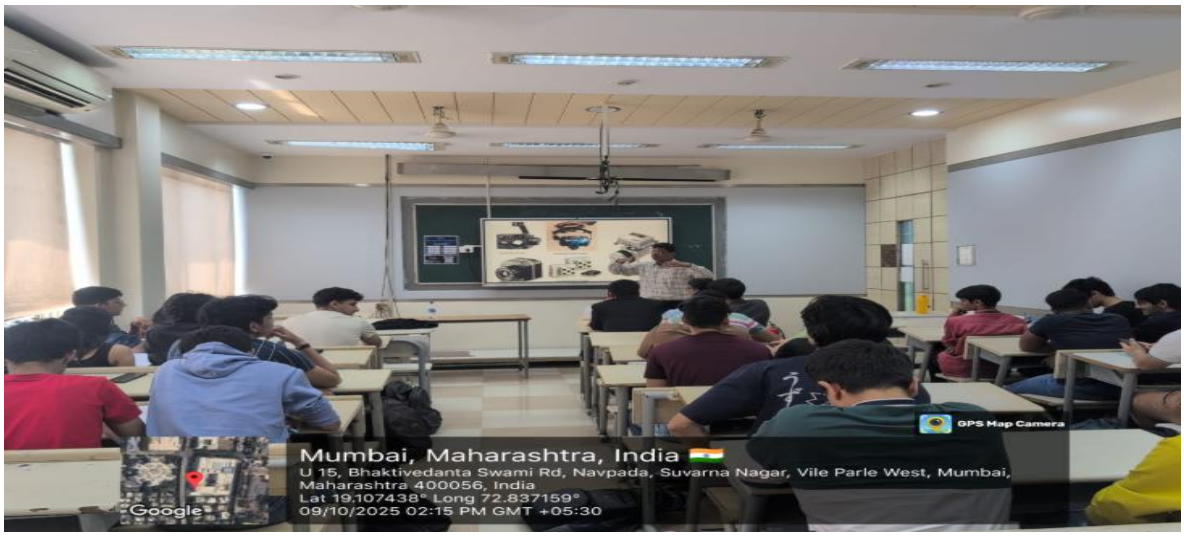
speaker included every branch of engineering by stating the importance of each one in the building and working of drones.

QUESTIONS AND ANSWERS:

Here students asked their doubts about this field. Some of the answers they received were that by pursuing M.Tech and specializing in areas like swarm technology or military drones can open up high-paying roles, with salaries starting at around ₹15 LPA for skilled professionals considering one knows skills like MATLAB. The SWAYAM portal was recommended as a valuable platform for learning about UAVs. Furthermore, to get corporate jobs in the field of UAV technology one needs to crack GATE, obtain a drone flying license, and consider applying for a Junior Research Fellowship (JRF) at IIT Powai. A creative personal project idea was also proposed—to mimic the sound signatures of various birds and create a comprehensive database from them.

EVENT PICTURES:

Department of Electronics and Telecommunication



Department of Electronics and Telecommunication

ACKNOWLEDGEMENTS:

The success of the EXTC Department Alumni Meet was made possible by the dedicated efforts of the faculty and organizing team. A special thank you to Prof. Ranjushree Pal (Alumni Coordinator) for her leadership in planning and executing the event, and to Dr. Amit Deshmukh, Head of the EXTC Department, for his unwavering support and encouragement. We also extend our gratitude to all the alumni who took the time to attend and share their valuable experiences, both in person and online.

IMPACT:

This session provided a clear understanding of the career paths and technical skills required in the rapidly growing UAV and drone industry. Students gained practical insights into drone anatomy, flight mechanisms, and advanced technologies like swarm and stealth systems. This session sparked curiosity among the young minds to explore this field further and gave them a clear path forward.

Dr. Anuja A Odhekar
Associate Professor,
Branch Counsellor,
IETE-ISF, DJSCE, Mumbai

Prof. Amit A. Deshmukh
Prof. & Head, Department of
Electronics and Telecommunications
Engineering, DJSCE, Mumbai

Department of Electronics and Telecommunication

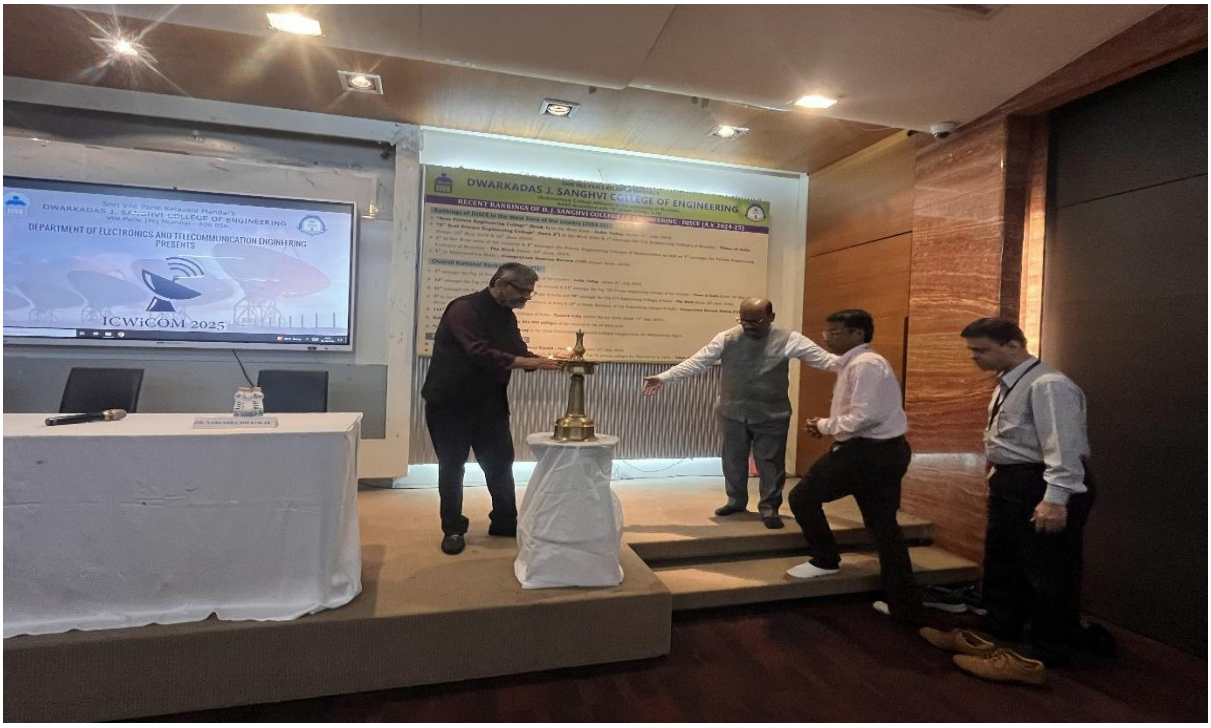
4.5 ICWICOM 2025

- Date- 10th October and 11th October 2025
- Venue- DJSCE
- Time- 9 a.m. - 5:30 p.m.

EVENT PROCEEDINGS:

Department of Electronics and Telecommunication Engineering at D. J. Sanghvi College of Engineering, Mumbai organised the International Conference on Wireless Communication (ICWiCOM) on 10th and 11th October, 2025 with the objective of promoting research and innovation in the field of wireless communication at the institute. The conference serves as a platform for idea exchange**,** technical discussions**,** and exposure to emerging technologies**,** bringing together eminent experts, researchers, academicians, and industry professionals from domains of antenna and microwave design**,** networking & signal processing**,** embedded systems and the Internet of Things (IoT)**,** Telemedicine and Image/Signal Processing for Wireless Applications. Overall, ICWiCOM provides a valuable platform to share advancements, discuss practical applications, and strengthen the research ecosystem in wireless communication.

EVENT PICTURES:



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Proceedings of International Conference on Wireless Communication

ICWiCom 2025

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Accessibility Information

Overview

Editors: Zoran Gajic, Hari Vasudevan, Amit A. Deshmukh, Valentina Emilia Balas, Marius M. Balas

- Presents research works in the field of wireless communication
- Provides best selected papers presented at ICWiCOM 2025
- Serves as a reference for researchers and practitioners in academia and industry

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Department of Electronics and Telecommunication

4.6 SUDHAGAD Trek under IETE-SF

- Date- 2nd November 2025
- Venue- Sudhgad fort
- Time- 5:00 a.m. – 10:00 p.m.

OBJECTIVE:

The Sudhagad Trek was organized to:

- Foster teamwork, resilience, and appreciation for nature.
- Offer an educational and adventurous experience beyond academics.
- Encourage mindfulness and social responsibility through community service.

CONTENT:

On 2nd November 2025, the IETE Students' Forum (ISF) and the Department of Electronics and Telecommunication Engineering (EXTC), Dwarkadas J. Sanghvi College of Engineering (DJSCE), organized a one-day trek to Sudhagad Fort. Conducted as a *trek for a cause*, the event included a donation of study materials to a local village school, combining adventure with a meaningful act of community service.

EVENT PROCEEDINGS:

The participants assembled early in the morning at Vile Parle Station at 5:00 a.m., followed by a pick-up stop at Vashi Plaza at 6:25 a.m. The journey to Sudhagad began soon after, with students traveling together by bus. The group reached the base camp around 10:00 a.m., marking the start of an exciting and refreshing day.

Before beginning the trek, the students and faculty members made a donation of books and stationery supplies to the local school near the base village — a thoughtful initiative to support the education of underprivileged children in the area.

The trek commenced at 10:30 a.m., offering participants a scenic yet challenging climb through lush greenery, rocky paths, and panoramic views. The team took short breaks along the way, engaging in conversations, capturing moments, and encouraging one another.

After reaching the fort and exploring its surroundings, the group paused for lunch at around 3:00 p.m. (participants carried their own meals). The descent began at 6:00 p.m., concluding a fulfilling and adventurous trekking experience.

Following the trek, the team travelled to Pali village, where they visited the Shree Ballaleshwar Ganapati Temple, one of the revered Ashtavinayak temples of Maharashtra. Later, everyone enjoyed dinner together at Sukh Sagar Restaurant, reflecting on the memorable day.
After dinner, the group departed from Pali and reached Vile Parle Station around 1:00 a.m., bringing the event to a close.

Department of Electronics and Telecommunication

EVENT PICTURES:

IETE Students' Forum at the Summit of Sudhagad Fort

Panoramic View from Sudhagad Fort

Donation at Sudhagad Base Village School

Department of Electronics and Telecommunication

ACKNOWLEDGEMENTS:

The successful completion of the Sudhagad Trek was made possible through the collaborative efforts of the Department of Electronics and Telecommunication Engineering and the IETE Students' Forum (ISF). We express our heartfelt gratitude to Dr. Amit A. Deshmukh, Prof. & Head, Department of Electronics and Telecommunication Engineering, for his invaluable guidance and constant support. We also extend our sincere thanks to the accompanying faculty members — Prof. Ankita Malhotra, Prof. Dipti Kale, and Prof. Abhilasha Raghtate — for their encouragement, supervision, and enthusiastic participation throughout the trek.

IMPACT:

The Sudhagad Trek offered students a unique blend of adventure, physical activity, and social engagement. It provided a refreshing break from academics while fostering endurance, camaraderie, and appreciation for nature.

The initiative to donate books and stationery to the local school added a meaningful dimension to the event, instilling in students the importance of community service and gratitude.

Overall, the trek was a resounding success — an experience that encouraged students to step outside their comfort zones, connect with their peers and mentors, and return with lasting memories and a renewed sense of purpose.

Dr. Anuja A Odhekar
Associate Professor,
Branch Counsellor,
IETE-ISF, DJSCE, Mumbai

Prof. Amit A. Deshmukh
Prof. & Head, Department of
Electronics and Telecommunications
Engineering, DJSCE, Mumbai

Department of Electronics and Telecommunication

4.7 Board of Studies Meeting

Minutes of the 11th BOS meeting held on 15th November, 2025

The Board of Studies meeting of the Department of Electronics and Telecommunication Engineering was conducted in a hybrid mode on Saturday, 15th November 2025, at 2:00 p.m. onwards in the conference room at DJSCE.

The meeting was held to discuss and approve:

1. Minutes of 10th BOS meeting for approval.
2. Content revision of semester V subject, "Fundamentals of Wave Theory and the RF Design" for discussion and approval.
3. Detailed syllabus for the semester VI Honors program of the DJS23 scheme for discussion and approval.
4. Examiner panel of all the B. Tech examinations to be conducted from Jan 2026 onwards for various subjects for approval.
5. Examiner panel for M. Tech examinations to be conducted from Jan 2026 onwards for the DJS24 scheme and Appointment of examiner for the Second Year M. Tech. Student for Dissertation Stage II, for examination to be held in even semester April – May 2026.

The meeting was attended by Principal Dr. Hari Vasudevan, BOS members Dr S. Mande, Dr Jaykrisnan Nair, Prof. K. P. Ray, Dr Sunil Kumar Kopparapu, Mr Sumit Ranka and faculty members of the EXTC Department.

The following were the points discussed and the suggestions provided: --

(i) Minutes of meeting of 10th BOS meeting were approved.

(ii) Content revision of semester V subject, "Fundamentals of Wave Theory and the RF Design" was presented by Dr. Amit Deshmukh and subsequently approved by the BoS members.

(iii) The UG DJS23 detailed scheme and syllabus for Honors degree for semester VI were presented for discussion and approval.

(iv) The suggestions made in the proposed syllabus of DJS23 UG curriculum are as follows:

In the subject "Deep Learning" (AIML Honors), Dr Jaykrisnan Nair suggested to

a) include an introduction to reinforcement learning and a large language model.

b) Dr Sudhakar Mande suggested to include impact of scaling of MOSFET on analog circuit

design in the subject "Analog VLSI" (VLSI Design honors). Also, he suggested to include "CMOS Analog Circuit Design" by P. E. Allen and D. R. Holberg as textbook instead of reference book.

iv) Examiner panel for UG curriculum and PG program was presented and approved by the committee.

v) Examiner panel for the Second Year M. Tech. Dissertation Stage II to be held in even semester April – May 2026 was presented and Dr. S. S. Kakatkar was appointed as an external examiner for the same.

The meeting concluded with vote of thanks to all the members present in the meeting.

Meeting Recording Link:

Recap: 11th BOS Meeting 15th Nov. 2025 Saturday, November 15 | Meeting | Microsoft Teams

Prof. Sheeja Nair
Autonomy Coordinator,
EXTC Dept., DJSCE

Dr. Poonam Kadam
Autonomy Coordinator,
EXTC Dept., DJSCE

Prof. Amit A. Deshmukh
Professor & Head,
EXTC Dept., DJSCE

4.8 Pre-Placement Activities

The goal of these activities is to improve the employability of final-year and pre-final-year students by organizing a series of pre-placement events. These activities are designed to provide students with the skills, knowledge, and confidence they need to succeed in campus placement drives and land their dream jobs.

These activities include:

1. Skill Development Workshops (Technical and Soft Skills)

Based on the feedback received from the alumni and the industrial experts, these activities were proposed and planned by the Faculty Placement Coordinators of the Electronics and Telecommunication Department Dr. Aarti G. Ambekar and Prof. Tushar Sawant, along with the Student's Placement Coordinators under the guidance of Prof. Amit A. Deshmukh (Prof. and Head EXTC Department) and Dr. Rajendra Khavekar (TPO, DJSCE).

One of the activities conducted in the first half of AY 2025-2026 was Session on Object Oriented Programming. The in-depth reports of the same is given below.

Sessions on *Object Oriented Programming*

Speaker: Prof. Nancy Nadar

Association of the Speaker: Assistant Professor, Department of Computer Engineering, DJSCE, Mumbai

Dates of the Sessions: 7th October 2025.

Mode of Conduct: Online

No. of Participants: 100+ Participants (Third Year & Final Year Students)

This session was introduced as a discussion on Object-Oriented Programming (OOP). The speaker, Prof Nancy Nadar, assistant professor in the computer department, has extensive experience in the field of OOPS and various other programming languages such as C/C++, Java, Python, etc. She has a master's degree and has industry experience in the said topic. The primary goal of the session was to cover the basics of Object-Oriented Programming [OOPs] and explore their practical applications in the industry.

Covering overview of Object-Oriented Programming (OOP) in Java Topics:

Prof. Nancy Nadar delivered an insightful overview of key Object-Oriented Programming [OOPs] concepts, focusing on their practical relevance in real-world scenarios. She emphasized

the importance of mastering the underlying logic behind OOPS, rather than being restricted by programming languages. The discussion covered versatile topics and foundation of OOPS concepts such as encapsulation, inheritance, polymorphism, etc. and their implementations, all aimed at enhancing problem-solving skills. Some of the topic that were covered were as follows:

Here's an overview of Object-Oriented Programming (OOP) in Java in simplified points:

- *Encapsulation*
  - Bundles data (attributes) and methods (functions) into a single unit (class).
  - Controls access to data through access modifiers (private, public), using getter and setter methods.
  - Helps protect data integrity and improve modularity.
- *Inheritance*
  - Enables new classes to inherit features (fields and methods) from existing classes.
  - *Promotes code reusability by allowing a subclass to extend a superclass.*
  - Uses the extends keyword to establish relationships between classes (e.g., classBike extends Vehicle).
- *Polymorphism*
  - Allows objects to be treated as instances of their parent class, improving flexibility.
  - Achieved through:
    - Method Overloading: Multiple methods with the same name but different parameters within the same class.
    - Method Overriding: A subclass provides a specific implementation for a method already defined in the superclass.
- *Abstraction*
  - Hides unnecessary implementation details, focusing only on essential features.
  - Achieved through:
    - Abstract Classes: Classes that can't be instantiated and often have abstract methods.
    - Interfaces: Define a contract for classes to implement, ensuring specific methods are included without detailing how they work.
- *Method Overriding*
  - Method overriding is used in runtime polymorphism. When a child class

overrides a parent class's method, the child class might offer an alternative implementation.

- *Method Overloading*
  - Method overloading is used in Compile Time Polymorphism. Although two methods or functions may have the same name, the number of arguments given into the method call may vary. Therefore, depending on the number of parameters entered, you may obtain different results.

Together, these principles create a structured, maintainable, and reusable approach to programming in Java, C++ and various different Object-Oriented Programming languages. The session on Object Oriented Programming [OOPs] led by Prof. Nancy Nadar concluded with a strong emphasis on practical understanding and real-world applications. Engaging around 150 students, Prof. Nancy underscored the significance of focusing on logical reasoning rather than getting bogged down by language-specific implementations. Through examples of explaining a class as a family to explain the hierarchy of a parent and a child class also through this example she explained method overloading and overriding—she made complex concepts accessible and relatable. Her encouragement for students to learn from others' solutions and gradually take on more challenging problems left them inspired to pursue continuous improvement in their academic and professional end devours. Overall, the session was a valuable experience, equipping students with the tools and mindset needed for success in the field of OOPs.

5. ACHIEVEMENTS

5.1 Faculty Publications- Conferences / Journals

Conference publication

Sr. No	First Author	Paper Details	Indexed by
1	Dr. Amit A. Deshmukh	Deshmukh, A.A. *et al.* (2025). Variations of Regular Shape Microstrip Antennas Loaded with Shorting Posts and Slots for Reduction in Cross Polar Levels. In: Gajic, Z., Vasudevan, H., Deshmukh, A.A., Balas, V.E., Balas, M.M. (eds) Proceedings of International Conference on Wireless Communication. ICWiCOM 2025. Lecture Notes in Electrical Engineering, vol 1499. Springer, Singapore. https://doi.org/10.1007/978-981-95-3616-0_24	Springer/ Scopus
2	Dr. Amit A. Deshmukh	Deshmukh, A.A. *et al.* (2025). Wideband Design of 110° Isosceles Triangular Microstrip Antenna Using Bow-Tie Ground Plane Profile. In: Gajic, Z., Vasudevan, H., Deshmukh, A.A., Balas, V.E., Balas, M.M. (eds) Proceedings of International Conference on Wireless Communication. ICWiCOM 2025. Lecture Notes in Electrical Engineering, vol 1499. Springer, Singapore. https://doi.org/10.1007/978-981-95-3616-0_23	Springer/ Scopus
3	Dr. Amit A. Deshmukh	Amit A. Deshmukh, Jainam Shah, Pratham Soneria, Sairudra Gudur, Mihir Sanghvi, Venkata A. P. Chavali, "Circularly Polarized Design Of Resonant V-slot Cut Square Microstrip Antenna", Accepted for publication in Proceedings of OWT 2025, 18th & 19th December 2025, NIT Goa, India, SPIE Proceedings.	Scopus
4	Dr. Amit A. Deshmukh	Amit A. Deshmukh, Shashank Naik, Yash Doke, Rahul Singhal, Mihir Sanghvi, Venkata A. P. Chavali, "Circularly Polarized Electromagnetically Coupled Stacked Variation of Corner Truncated Square Microstrip Antennas", Accepted for publication in Proceedings of OWT 2025, 18th & 19th December 2025, NIT Goa, India, SPIE Proceedings.	Scopus
5	Prof. Yukti Bandi,	Bandi, Y., Joshi, P. (2025). Electroencephalogram Based Imagined Digit Classification. In: Gajic, Z., Vasudevan, H., Deshmukh, A.A., Balas, V.E., Balas, M.M. (eds) Proceedings of International Conference on Wireless Communication. ICWiCOM 2025. Lecture Notes in Electrical Engineering, vol 1499. Springer, Singapore. https://doi.org/10.1007/978-981-95-3616-0_12	Springer/ Scopus
6	Dr. Supriya Dicholkar	Dicholkar, S., Mohadikar, P., Pandya, M., Nair, P., Shriyan, D. (2025). Smart Living: A Comprehensive Framework for IoT-Based Home Automation. In: Gajic, Z., Vasudevan, H., Deshmukh, A.A., Balas, V.E., Balas, M.M. (eds) Proceedings of International Conference on Wireless Communication. ICWiCOM 2025. Lecture Notes in Electrical Engineering, vol	Springer/ Scopus

		1499. Springer, Singapore. https://doi.org/10.1007/978-981-95-3616-0_19	
7	Prof. Sheeja Nair	Nair, S., Karamchandani, S., Venkataramanan, V. (2025). HDL-Compatible Modeling of 1024-QAM MIMO SC-FDMA/OFDMA Systems with Convolutional Encoder and Viterbi Decoder in LTE-A and 5G NR NSA. In: Gajic, Z., Vasudevan, H., Deshmukh, A.A., Balas, V.E., Balas, M.M. (eds) Proceedings of International Conference on Wireless Communication. ICWiCOM 2025. Lecture Notes in Electrical Engineering, vol 1499. Springer, Singapore. https://doi.org/10.1007/978-981-95-3616-0_11	Springer/ Scopus
8	Prof. Chandrashekhar Beral	Beral, C.K., Tibdewal, M.N. (2025). Design Priority Based Congestion Management in Wireless Sensor Networks with Bacterial Foraging Optimizer and Q-Learning. In: Gajic, Z., Vasudevan, H., Deshmukh, A.A., Balas, V.E., Balas, M.M. (eds) Proceedings of International Conference on Wireless Communication. ICWiCOM 2025. Lecture Notes in Electrical Engineering, vol 1499. Springer, Singapore. https://doi.org/10.1007/978-981-95-3616-0_13	Springer/ Scopus
9	Prof. Mrunalini Pimpale	Pimpale, M., Joshi, P. (2025). Time-Frequency and 2-Dimensional Spectral Domain Feature Extraction of Lung Sound. In: Gajic, Z., Vasudevan, H., Deshmukh, A.A., Balas, V.E., Balas, M.M. (eds) Proceedings of International Conference on Wireless Communication. ICWiCOM 2025. Lecture Notes in Electrical Engineering, vol 1499. Springer, Singapore. https://doi.org/10.1007/978-981-95-3616-0_16	Springer/ Scopus
10	Prof. Tushar Sawant	Sawant, T., Doshi, M., Jha, P. (2025). Train Management System. In: Gajic, Z., Vasudevan, H., Deshmukh, A.A., Balas, V.E., Balas, M.M. (eds) Proceedings of International Conference on Wireless Communication. ICWiCOM 2025. Lecture Notes in Electrical Engineering, vol 1499. Springer, Singapore. https://doi.org/10.1007/978-981-95-3616-0_17	Springer/ Scopus
11	Prof. Pavankumar Borra	Borra, P. (2025). Data-Driven Vehicle Autonomy: A Comprehensive Review of Sensor Fusion, Localisation, and Control. In: Gajic, Z., Vasudevan, H., Deshmukh, A.A., Balas, V.E., Balas, M.M. (eds) Proceedings of International Conference on Wireless Communication. ICWiCOM 2025. Lecture Notes in Electrical Engineering, vol 1499. Springer, Singapore. https://doi.org/10.1007/978-981-95-3616-0_25	Springer/ Scopus

Journal publication

Sr. No	First Author	Paper Details	Indexed by
1	Prof. Amit A. Deshmukh	Venkata A. P. Chavali, Amit A. Deshmukh, "Shorted Microstrip Line Fed Wideband Design of E-Shape Microstrip Antenna Loaded with Printed Rectangular Resonator", Progress in Electromagnetics Research C, Vol. 163, pp. 81 – 90, 2026 (https://www.jpier.org/issues/volume.html?paper=25101901, doi:10.2528/PIERC25101901).	Scopus
2	Prof. Amit A. Deshmukh	Venkata A. P. Chavali, Amit A. Deshmukh, "Thinner Substrate Wideband Designs of Proximity Fed Rectangular Microstrip Antennas For GSM Band applications", International Journal of Microwave and Wireless Technology, pp. 1 – 11, 2026, Cambridge Publication, (DOI: https://doi.org/10.1017/S1759078725102754).	Scopus
3	Prof. Amit A. Deshmukh	Amit A. Deshmukh, Spoorthi Shetty, Jash Furia, Nidhi Gandhi, "Circular Microstrip Antenna Loaded With Shorting Posts and Sectoral Slots For Lower Cross-Polar Radiation", Accepted for publication in Journal of Microwaves, Optoelectronics and Electromagnetic Applications.	Scopus
4	Prof. Amit A. Deshmukh	Amit A. Deshmukh, Venkata A. P. Chavali, Aarti G. Ambekar, "Isosceles Triangular Microstrip Antenna Against Varying Angle For Circular Polarized Response", International Journal of Microwave and Optical Technology, Vol. 20, no. 5, pp. 508 – 515, September 2025.	Scopus
1	Prof. Mrunalini Pimpale	V, Venkataramanan, Mrunalini Pimpale, Vijay Kapure, Pankaj Mishra, Aarya Rokade, Tulsi Bhushan, and Jitendra Singh. 2025. "A Hybrid IoT and Machine Learning Framework for Smart Greenhouse Automation in Sustainable Agriculture". *International Research Journal of Multidisciplinary Technovation* 7 (4):58-69. https://doi.org/10.54392/irjmt2545.	SCIE /SSCI
2	Prof. Archana Chaudhari	Chaudhari A, Mahajan A, Nainan S, Shah D, Noronha C. Selection of human embryo for IVF treatment using ensemble machine learning technique. Morphologie. 2025 Nov 18;110(368):101082. doi: 10.1016/j.morpho.2025.101082. Epub ahead of print. PMID: 41260181.	Scopus, SCI

Book publication

Sr. No	**Name of Faculty**	**Title of the Book**	**Publisher's Name**	**Year of Publication**
1	Prof. Amit A. Deshmukh, Dr. Aarti G. Ambekar	Neural Network Modelling of Microstrip Antennas	Springer Singapore	SPRINGER Oct-25

5.2 Interaction of faculty with outside world

FDP/ STTP/Webinar/Workshop attended by Faculty Members:

Sr. No.	Name Of Faculty	Details of Workshop/ Webinar/STTP/FDP	Date / Year of Event
1	Dr. Satishkumar Chavan	Attended IIC Regional Meet 2025, MoE's Innovation cell Institutions Innovation Council, AICTE organized by SVKM's DJSCE.	2nd December 2025
2	Dr. Sunil Karamchandani	Attended IIC Regional Meet 2025, MoE's Innovation cell Institutions Innovation Council, AICTE organized by SVKM's DJSCE.	2nd December 2025
3	Dr. Poonam Kadam	Attended IIC Regional Meet 2025, MoE's Innovation cell Institutions Innovation Council, AICTE organized by SVKM's DJSCE.	2nd December 2025
4	Dr. Poonam Kadam	Attended Workshop on Academic Quality Enhancement: A Forward Path organized by NMIMS in collaboration with N.M. College of Commerce, D.J. Sanghvi College of Engineering, & Jitendra Chauhan College of Law, facilitated by Dr. N. Jayasankaran	26th and 27th November 2025
5	Dr. Anuja A Odhekar	workshop on "Antenna Technologies for Space Applications"	14th October 2025
6	Dr. Anuja A Odhekar	Attended IIC Regional Meet 2025, MoE's Innovation cell Institutions Innovation Council, AICTE organized by SVKM's DJSCE.	2nd December 2025
7	Dr. Aarti G. Ambekar	FDP on AICTE Training And Learning (ATAL) on Integrating AI, IoT, and Adaptive Antennas for HighPerformance Communication Systems at ST. JOHNS COLLEGE OF ENGINEERING & TECHNOLOGY	15th September to 20th September 2025
8	Dr. Aarti G. Ambekar	Participated & completed AICTE Training And Learning (ATAL) Academy Faculty Development Program on SEMI-TECH: Semiconductor Innovation & Technology for Next-Gen Electronics at SRM Institute of Science and Technology	18th to 23rd August 2025
9	Dr. Aarti G. Ambekar	Completed a One week FDP on "Smart Biomedical Signal Processing: Leveraging IoT, Edge Computing, and ML" organized by EICT Academy IIT Roorkee.	12th July to 16th July 2025
10	Dr. Aarti G. Ambekar	Completed a One week FDP on "Recent Trends in AI applications for Microwave Engineering" organized by EICT Academy NIT Patana	7th July to 11th July 2025
11	Dr. Aarti G. Ambekar	Attended webinar on The AI Driven Future Smart Cyber Space Security ",organized by SCHOLARSCOLAB in association with IEEE	6th December 2025

		MTT-S Society ABV-IIITM Gwalior MP Section/CH11187	
12	Rahul Taware	Completed Industrial Training on Internet of Things	06 week (1st July to 16th August 2025)
13	Revathi A S	(ATAL) FDP on Blue and Green Economies: Integrated Approaches for Sustainable Futures	19th September to 25th September 2025
14	Prof.Abhilasha Raghtate	Completed FDP on Creative Thinking: Techniques and Tools for Success	10th July 2025
15	Prof.Abhilasha Raghtate	Completed FDP on Foundations of Teaching for Learning: Curriculum	9th July 2025
16	Prof.Abhilasha Raghtate	Attended IIC Regional Meet 2025, MoE's Innovation cell Institutions Innovation Council, AICTE organized by SVKM's DJSCE.	2nd December 2025
17	Prof. Supriya Dicholkar	successfully completed Foundations of Cybersecurity an online non-credit course authorized by Google and offered through Coursera.	11th July 2025
18	Prof. Supriya Dicholkar	successfully completed Foundations of Teaching for Learning: Curriculum an online non-credit course authorized by Commonwealth Education Trust and offered through Coursera	9th July 2025
19	Prof. Supriya Dicholkar	successfully completed University Teaching an online non-credit course authorized by The University of Hong Kong and offered through Coursera	5th July 2025
20	Prof. Supriya Dicholkar	successfully completed AI For Everyone in online non-credit course authorized by DeepLearning.AI and offered through Coursera	3RD July 2025
21	Dr. Supriya Dicholkar	participated and successfully completed the Six Day ' s Faculty Development Program on "Insights into Research Methodology and Publication Ethics " organized by Research And Development Cell-TSEC	18th to 23rd August 2025
22	Prof. Supriya Dicholkar	completed Innovation Ambassador foundation level by AICTE Innovation Cell	2nd August 2025
23	Dr. Supriya Dicholkar	Attended ISTE approved STTP on Network Security: Concepts, Protocols and Practical Implementation organized by FCRIT, Vashi	8th – 12th December 2025
24	Dr. Supriya Dicholkar	Attended IIC Regional Meet 2025, MoE's Innovation cell Institutions Innovation Council, AICTE organized by SVKM's DJSCE.	2nd December 2025
25	Dr. Ankita Malhotra	Attended IIC Regional Meet 2025, MoE's Innovation cell Institutions Innovation Council, AICTE organized by SVKM's DJSCE.	2nd December 2025

26	Prof. Dipti Kale	successfully completed Foundations of Cybersecurity an online non-credit course authorized by Google and offered through Coursera.	11th July 2025
27	Prof. Dipti Kale	successfully completed Foundations of Teaching for Learning: Curriculum an online non-credit course authorized by Commonwealth Education Trust and offered through Coursera	9th July 2025
28	Prof. Dipti Kale	successfully completed University Teaching an online non-credit course authorized by The University of Hong Kong and offered through Coursera	5th July 2025
29	Prof. Dipti Kale	successfully completed AI For Everyone an online non-credit course authorized by DeepLearning.AI and offered through Coursera	3rd July 2025
30	Prof. Dipti Kale	Attended IIC Regional Meet 2025, MoE's Innovation cell Institutions Innovation Council, AICTE organized by SVKM's DJSCE.	2nd December 2025
31	Dr. Santoshkumar Sabat	successfully completed AI For Everyone an online non-credit course authorized by DeepLearning.AI and offered through Coursera	25th July 2025
32	Dr. Santoshkumar Sabat	successfully completed University Teaching an online non-credit course authorized by The University of Hong Kong and offered through Coursera	24th July 2025
33	Dr. Santoshkumar Sabat	successfully completed Understanding Research Methods an online non-credit course authorized by University of London and SOAS University of London and offered through Coursera	18th July 2025
34	Dr. Santoshkumar Sabat	successfully completed Creative Thinking: Techniques and Tools for Success an online non-credit course authorized by Imperial College London and offered through Coursera.	22nd July 2025
35	Prof. Renia Dias	Completed FDP on Technical Communication	July 2025
36	Prof. Renia Dias	Completed one-week FDP on Ethical and Responsible AI: Harnessing XAI for India's Economic Future	14TH July to 19th July 2025
37	Prof. Renia Dias	Completed FDP on relative Thinking: Techniques and Tools for Success an online non-credit course authorized by Imperial College London and offered through Coursera	July 2025
38	Prof. Renia Dias	Attended IIC Regional Meet 2025, MoE's Innovation cell Institutions Innovation Council, AICTE organized by SVKM's DJSCE.	2nd December 2025

5.3 NPTEL/COURSERA Courses completed by faculty members:

Sr.No	Name Of Faculty	Details of Workshop/ Webinar/STTP/FDP	Date / Year of Event
1	Dr. Ameya A. Kadam.	NPTEL FDP course on Accreditation and Outcome Based Learning completed with silver medal.	July to November 2025 (8 week)
		NPTEL FDP course on OBE and Accreditation completed with Topper + Gold Medal.	July to November 2025 (12week)
		NPTEL FDP course on OBE and Accreditation completed with Topper + Gold Medal.	July to November 2025 (12 week)
2	Dr. Satishkumar Chavan	NPTEL FDP on Medical Image Analysis.	July to November 2025 (12week)
3	Dr. Anuja A Odhekar	NPTEL FDP on Nanophotonics, Plasmonica and Metamaterials	July to November 2025 (12week)
4	Prof. Yukti Bandi	NPTEL FDP on Machine learning	July to November 2025 (12week)
5	Prof. Sejal A. Kadam	NPTEL FDP course on OBE and Accreditation completed with Topper + Gold Medal.	July to November 2025 (12week)
		NPTEL FDP on Real-Time Digital Signal Processing with Topper + Silver Medal.	July to November 2025 (12week)
6	Abhilasha Raghtate	NPTEL FDP course on "Research Methodology" with Elite Silver grade	July to Sept 2025
		NPTEL Course on Artificial Intelligence: Concepts and Techniques	July-Oct 25
		NPTEL Course on Solar Photovoltics Fundamental Techniques and Applications	July-Oct 25

NPTEL DISCIPLINE STAR

CERTIFICATE OF APPRECIATION

TO

MS BAHAR CHETAN SOPARKAR

Computer Science and Engineering

for being recognized as NPTEL DISCIPLINE STAR

JUL-DEC 2025

Prof. Andrew Thangaraj
Chair
Centre for Outreach and Digital Education, IITM

Prof. Vignesh Muthuvijayan
NPTEL Coordinator
IIT Madras

NPTEL DISCIPLINE STAR
Candidate has to be certified in courses of same discipline, completed more than 50 weeks of learning, final score in each subject>=55

NPTEL swayam

5.4 Faculty Achievements

Name of Faculty	Event description	Date
Prof. Amit A. Deshmukh	Served as external evaluator for Mock NBA preparation visit to LRTCE, Mira road, for assessing EXTC Department preparation	
	Invited as External examiner for APS assessment at KJSIET, Sion, Mumbai	
	Worked as BOS committee for RCPIT, Shirpur	
	Worked as VC nominee on BOS of Mechatronics Department at TCET, Mumbai	
	Served as reviewer for Journals like, International Journal of Communication Systems, International Journal of Antennas and Propagation, Progress in Electromagnetic Research, International Journal of RF and Microwave Computer-Aided Engineering, AEU International Journal of Electronics and Communication Engineering, Journal of Electrical and Computer Engineering.	
Dr. Prasad S. Joshi	Invited for selection panel member at "University Staff Selection Committee" process, as subject expert, for the post of Assistant Professor, in the department of Electronics & Computer Science, at TSEC(Thakur Shyamnarayan Engineering College, Thakur Complex, Kandivali East.	29th November 2025
	attended ' Automation Expo 2025' at NESCO Ground, Mumbai along-with students of TE & BE (EXTC)	14th August 2025
	Member Programme-wise Board of Studies for Department of Electronics and Telecommunications Engineering, Shri Bhagubhai Mafatlal Polytechnic on Friday.	1st August' 2025
	Invited for selection panel member at "University Staff Selection Committee" process, as subject expert, for the post of Assistant Professor, in the department of Electronics & Telecommunication Engineering and Internet of Things, at TCET, Thakur Village, Kandivali East.	17th July 2025
	Worked as member Domain Advisory Committee (DAC) for Topic Approval Seminar of Ph.D. Student, at Department of Electronics Engineering, K. J. Somaiya College of Engineering,	9th July 2025
	Invited to present the implementation of the concept - Ideation and Innovation Laboratory as mandatory course first year of engineering at the institute.in 35th Annual conference and exhibition on NDT evaluation and enabling technologies at Jio Convention Centre, Bandra, Mumbai	12th December 2025
	Invitation as subject expert - Electronics and Computer Engineering, Interview for post of Assistant Professor by Thakur Shyamnarayan Engineering College, Kandivali East	29th November 2025
Dr. Sunil karamchandani	worked as examiner in topic approval seminar in K J Somaiya College of Engineering.	September 2025
Dr. Anuja Odhekar	Appointment as an Expert for Exhibition cum ESE Mini Project 1 at Sardar Patel Institute of Technology, Andheri(W), Mumbai-58	26th November 2025

Dr. Aarti G Ambekar	recognized as a reviewer for IEEE International Conference on Artificial Intelligence, Computer, Data Sciences and Applications (ACDSA 2026), Philippines, for Bulletin of Electrical Engineering and Informatics by IAES, and for International journal of Communication System by Wiley Publications.	November 2025
	recognized as a peer reviewer for the International Journals IEEE access and International Journal of Communication Systems and 3rd International Conference on Artificial Intelligence, Computer, Data Sciences and Applications which will take place in Boracay Island, Philippines on 05-07 February 2026	October, 2025
	worked as editorial board member in a SPRINGER's International Journal scientific reports.	September 2025
	peer Reviewer for IEEE Access journal	
	Recognition as a peer reviewer for the international journal IEEE access.	August 2025.
	worked as a peer reviewer for THE JOURNAL IEEE Access and for THE JOURNAL INTERNATIONAL JOURNAL OF COMMUNICATION SYSTEMS IJCS	July 2025
	Recognition as a reviewer in Scientific journal Bulletin of Electrical Engineering and Informatics	10th December 2025
Prof. Rahul Taware	Worked as Question Paper setting by KJSCE University	8th December 2025
Dr. Darshan Sankhe	Appointment as an Expert for Exhibition cum ESE Mini Project 1 at Sardar Patel Institute of Technology, Andheri(W), Mumbai-58	26th November 2025
Dr. Supriya Dicholkar	as a reviewer for IEEE International Conference on Artificial Intelligence, Computer, Data Sciences and Applications (ACDSA 2026), Philippines.	November 2025
	worked as reviewer for 1st Taylor and Francis (Scopus) International Conference on Smart Systems for Sustainable Development using Advanced Computational Techniques (ICSSA 2025)	October 2025
	published design patent titled A smart wardrobe with patent number 20251077917	29th August 2025
	awarded with Ph. D. degree from K. J. Somaiya College of Engineering.	25th August 2025.
	Worked as mentor for 20th Avishkar final Round selected team for 20th Avishkar – UoM	10th December 2025
	Appointed as paper setter and moderator for analog and Digital Communication Sem V by St. Francis Institute of Technology	10th December 2025
	Appointment as an Expert for Exhibition cum ESE Mini Project 1 at Sardar Patel Institute of Technology, Andheri(W), Mumbai-58	26th November 2025
Prof. Vivek Nar	Appointment as an Expert for Exhibition cum ESE Mini Project 1 at Sardar Patel Institute of Technology, Andheri(W), Mumbai-58	26th November 2025

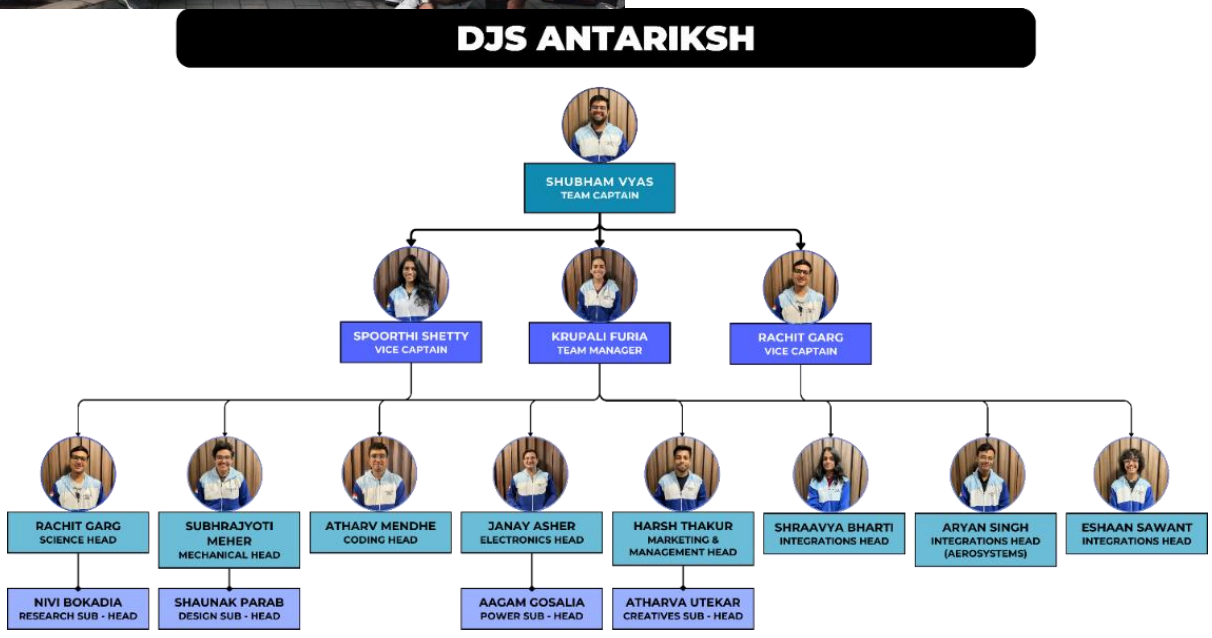
5.5 Student's participation in various events

Sr. No.	Student Name	Type of Event	Date	Award/ Achievement
1	Aadit Shah	MATLAB AI challenge 2025	Sept 2025	World ranking 1, 1000$ prize money
2	Avaneesh Chalke	The Synapse – Tech Debate	19th Sept 2025	First Position
3	Avaneesh Chalke	ACE 2.0 All coding Excellence Hackathon	6th Sep - 7th Sept 2025	Runner up
4	Varun Nitin Mutha	National Finalist in the Sociovision Challange conducted by Inceptio IEC(An Innovation and Entrepreneurship Cell) of NMIMS' Mukesh Patel School of Technology Management and Engineering, Mumbai	October 2025	Finalist
5	Rajat Viroja, Devansh Lad	Hands-on PCB Design Session workshop organized by DJS IEEE	18th and 19th October 2025	Participated
6	Hitanshi jain	Completed Nptel course on data science for engineers	4 Week course (JUL-SEPT 2025)	Completed Course
7	Ayushman Yadav	Completed Oracle OCI Course by Oracle	3 months	Test score: 80/100
8	Belishma Shah	Completed DSA in Java (Sigma 3.0-Alpha Batch) by Apna College (Shradha Khapra)	4 months	Completed Course
9	Jinansh Mehta	Completed Nptel course on data science for engineers	4 Week course (JUL-SEPT 2025)	Elite Certificate
10	Jinansh Mehta	Completed Nptel course on Python for data Science	4 Week course (JUL-SEPT 2025)	
11	kalash bheda	Won 1ST PRIZE IN HARDWARE SECTION AND 3RD OVERALL AT KJSIT : LEVEL UP in KJSCE :LEVEL UP , THAKUR COLLEGE : HACKNOVA competition		1ST PRIZE IN HARDWARE SECTION AND 3RD OVERALL AT KJSIT : LEVEL UP
12	AAKASH TAMBWEKAR	ROBOAI program from my equation, and pcb design workshop of IEEE,	1st November 2025	Participated
13	Krushna Sonawane	Introduction to Power Electronics – University of Colorado Boulder (Coursera).	2nd November 2025	Completed Course
14	Krushna Sonawane	Complete PLC Software/Hardware & Full Automation Bootcamp – Udemy.	2nd November 2025	Completed course
15	Shlok Gothi	Completed RoboAI course organized by My Equation	4th November 2025	Completed course
16	Shravani Pramod Rane	NPTEL Certification on Programming With Generative AI	15th November 2025	Completed 8 Weeks course
17	Krish Ramani	Smart India Hackathon 2025	9th December 2025	First Prize
18	Kulkarni Om	20th Avishkar- Inter-collegiate Research Convention UoM	9th December 2025	Selected for Final round
19	Shah Purva	20th Avishkar- Inter-collegiate	9th December	Selected for Final

		Research Convention UoM	2025	round
20	Dhabalia Palash	20th Avishkar- Inter-collegiate Research Convention UoM	9th December 2025	Selected for Final round
21	Seluker Maitreyi	20th Avishkar- Inter-collegiate Research Convention UoM	9th December 2025	Selected for Final round
22	Param Gandhi	FMAE MOTOSTUDENT INDIA National level Project Competitions at Coimbatore		Runner-ups in Autocross competition
23	JENIKA JAIN	Completed Internship at Company - Connector Devices (Internship)	15th June to 15th September 2025	
24	Jash Furia	Won in MALHAR Volleyball Tournament organized by Xavier's College, Churchgate	14th August 2025	3rd Place in competition

DJS Antariksh Team Introduction

DJS Antariksh is the official Martian Rover Team of Dwarkadas J. Sanghvi College of Engineering, Mumbai, affiliated with Mumbai University. Founded in 2019, the team operates under the motto **"To Decipher Unimaginable,"** reflecting its commitment to pushing the frontiers of space exploration through innovation. The team consists of 60 passionate second and third year undergraduate students from various engineering backgrounds, organized into five key departments: **Mechanical, Electronics, Coding, Science, as well as Marketing and Management.**

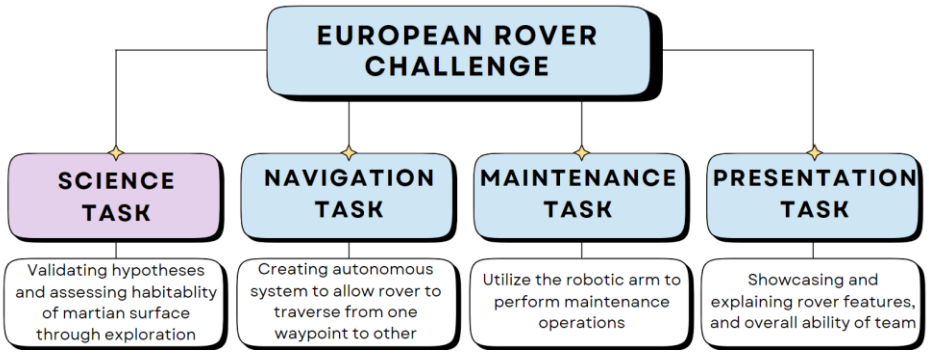


Competitions

1. European Rover Challenge

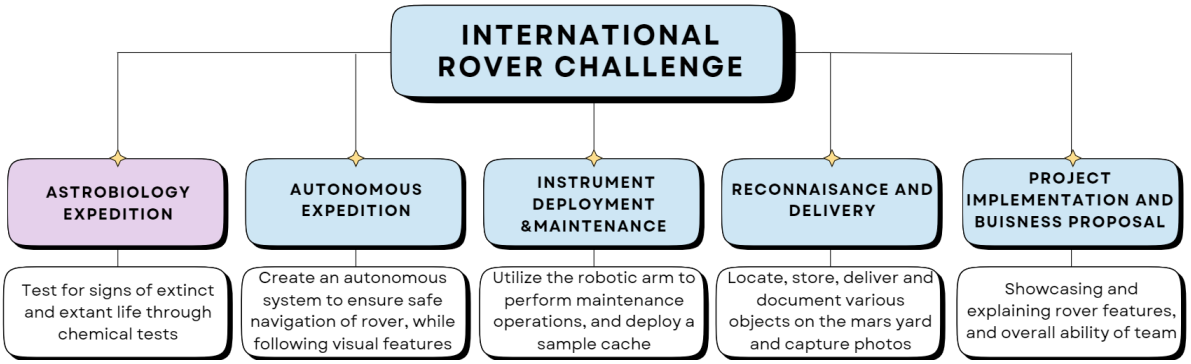
European Rover Challenge

The European Rover Challenge organized by the European Space Foundation takes place every year in Poland. It is an integrated programme working towards technological developments, specifically those in GPS-denied environments, with space exploration and utilization as the leading theme. The ultimate goal of the ERC is to become a standardized test trial and benchmark for planetary robotic activities, coupled with strong professional career development platform.. The event brings together university teams to design and operate Martian rover prototypes that are tested on a Mars-like terrain. The competition includes tasks such as autonomous navigation, astrobiology tasks, maintenance operations giving teams a practical platform to apply and test their engineering work. Over the years, the team's participation at ERC has helped steadily improve rover designs, strengthen technical approach, and build consistency in performance on the international stage. Through these achievements, the team has also been able to represent the college and bring recognition to it at a global level.



2. International Rover Challenge

The International Rover Challenge is an international competition organised by the Space Robotics Society. It challenges university students to conceptualise, design, develop and operate an astronaut-assistive next-generation space Rover. The objective of the competition is to provide students with a real-world interdisciplinary engineering experience, combining practical engineering skills with soft skills, including business planning and project management.



ERC On-site
Qualification:

In the ERC 2025 Qualification Round**,** DJS Antariksh secured 1st place worldwide, finishing at the top among 102 participating teams from multiple countries across the globe. This achievement qualified DJS Antariksh for the On-Site Finals in Poland**,** marking a proud moment for the team.

ERC 2025 Result

At the ERC 2025 On-Site Finals in Poland, DJS Antariksh secured 7th place worldwide**,** 1st in Asia and 1st in India reflecting steady growth and consistent performance in the competition over the years.

No.	Team's Name	Country	ERC FINAL SCORE (max 3000 pts)
1	EPFL Xplore	Switzerland	2180,4
2	STAR Dresden e.V.	Germany	2147,84
3	AGH Space Systems	Poland	2048,05
4	DIANA	Italy	1927,94
5	FHNW Rover Team	Switzerland	1801,9
6	Team Raptors PL	Poland	1770,3
7	DJS Antariksh	India	1743,5
8	SKA Robotics	Poland	1622,7
9	KNR Rover Team	Poland	1554,9
10	Mars Rover Manipal	India	1530,2

India's Aerospace Triumph: Team DJS Arya Shines at CanSat 2025

Team DJS Arya from Dwarkadas J. Sanghvi College of Engineering, Mumbai, achieved a global triumph at the prestigious International CanSat Competition 2025, organized by the American Astronautical Society (AAS) and NASA. Their journey, driven by the belief, "Success is no accident," cemented India's rising prominence in student-led space engineering.

Competing against 400 international teams, DJS Arya demonstrated unparalleled technical excellence and consistency across every critical stage:

- All India Rank 1
- Global Rank 5 in the Preliminary Design Review (PDR) with a score of 98.40%
- Critical Design Review (CDR): 98.45%
- Environmental Test Review (ETR): 100%,
- Flight Readiness Review (FRR): 100%,
- Post-Flight Review (PFR): Among the only 6 teams out of 40 to score above 90%
- Overall Score: 90.54% and Global Rank 15

The 2025 mission statement challenged the participants to design and build an Auto-Gyro Descender CanSat that stabilizes itself aerodynamically upon deployment. DJS Arya delivered a masterclass in system integration:

- Mechanical Subsystem: Designed for robust structural integrity and precise deployment of the Mechanisms.
- Electronics Subsystem: Featured a custom main PCB, and a telemetry system for real-time data transmission of the required data.
- Software Subsystem: Developed a custom Graphical User Interface (GUI) for live telemetry.
- Ground Station Antenna: A highlight was the in-house fabricated antenna, which received special praise from NASA and AAS judges for its design and performance.

Flight Performance and Impact

At the final launch in Monterey, Virginia, the CanSat successfully deployed from the sounding rocket at ≈700 meters, initiating its container-payload separation, activating its auto-gyro aided descent and transmitting vital telemetry to the GCS.

- Bonus Points: DJS Arya was one of the few teams to successfully record an in-flight video of the payload release mechanism.
- Honest Evaluation: Despite partial payload loss during recovery, their PFR presentation was lauded for its clarity and detailed analysis, securing their top position in that category.

Representing India among global powerhouses like Argentina, Turkey, and Canada, Team DJS Arya's indigenous designs, reliability, and perfect scores in ETR and FRR demonstrated India's growing technical competence in aerospace.
From late nights spent in brainstorming to finalizing a complete design to finalizing the best electronic components to telemetry tests in the Virginia hills, the team's journey was a testament to passion and teamwork. Securing All India Rank 1 and Global Rank 15, Team DJS Arya is not just a participant; they are an inspiration, laying down a powerful legacy of innovation for young Indian engineers and shining brightly on the world aerospace stage.

Team DJS Arya Conquers the National CanSat Stage

Team DJS Arya from Mumbai's Dwarkadas J. Sanghvi College of Engineering scripted history by clinching the First Rank in the InSpace CanSat India Competition 2024, organized by the Astronautically Society of India in collaboration with ISRO. This achievement, fueled by sheer hard work and determination, etched their name in the nation's space sector
The mission challenged participants to design and build a CanSat weighing under 1kg, capable of being launched to an apogee of 1000m. Upon separation, the CanSat was required to descend safely, maintain attitude stability about all three axes, and deploy a secondary descent mechanism.

Team DJS Arya's CanSat featured ingenious mechanisms:

- Stability: A Mechanical Gyro System was designed to stabilized the 3 axes during the descent
- Controlled Descent: A Secondary Parachute deployed automatically at 500 m altitude, reducing the descent rate for a smooth landing.
- Data Transmission: The Telemetry System enabled real-time transmission of data, including altitude, temperature, and attitude.

Team DJS Arya achieved a Near-Perfect Performance and these were the parameters which led them to victory.

- The launch was a complete success, with the CanSat reaching an altitude of 602m.
- Descent Rates: The CanSat could successfully achieve the ideal descent rates
- Equilibrium: A negligible Angular Momentum wasachieved, indicating a perfectly stabilized descent in equilibrium.
- Recovery: The CanSat was successfully retrieved within 10 minutes after landing.

Their interdisciplinary brilliance and preparation impressed InSpace Directors, who complimented them as an 'Advanced Team'. Furthermore, the team had the esteemed opportunity to meet remarkable personalities, including the Chief Guest, Group Captain Shubhansh Shukla (Indian Test Pilot and Astronaut).

Team DJS Arya's First Rank victory in the National InSpace CanSat India Competition 2024 was a momentous national achievement. Their ability to design and execute a complex mission with near-perfect results, demonstrating flawless stability and swift recovery, validated their comprehensive interdisciplinary approach. This triumph not only brought prestige to Mumbai but also served as a powerful validation of their hard work, proving they are a Team ready to contribute significantly to India's burgeoning space sector.

Runner-Up in Health & Wellness Domain – ACE 2.0 Hackathon

Avaneesh Sushant Chalke of Second Year, Electronics and Telecommunication Engineering (EXTC), From Dwarkadas J. Sanghvi College of Engineering, had the opportunity to participate in ACE 2.0 – All Coding Excellence Hackathon, organized by Mukesh Patel School of Technology Management & Engineering (MPSTME) on 6th and 7th September 2025. The event encouraged students to design innovative solutions across domains such as Health and Wellness Tech, Campus Solutions, Emotional Intelligence, and Smart Governance. It was conducted in two rounds—an online ideation and prototype round, followed by an offline build-and-present round.

Our team participated in the Health and Wellness Tech domain, where we developed a fully functional web-based application named Healix – Intelligent Health Platform, aimed at providing smart healthcare solutions. With creativity, technical expertise, and teamwork, our project stood out among many participants, and we secured the Runner-Up Position in our domain. We were awarded a trophy, certificates, and exclusive gift hampers as recognition of our efforts. This achievement not only strengthened our problem-solving and coding skills but also gave us the platform to apply our knowledge to real-world challenges, bringing pride to our department.

6 RESULT ANALYSIS

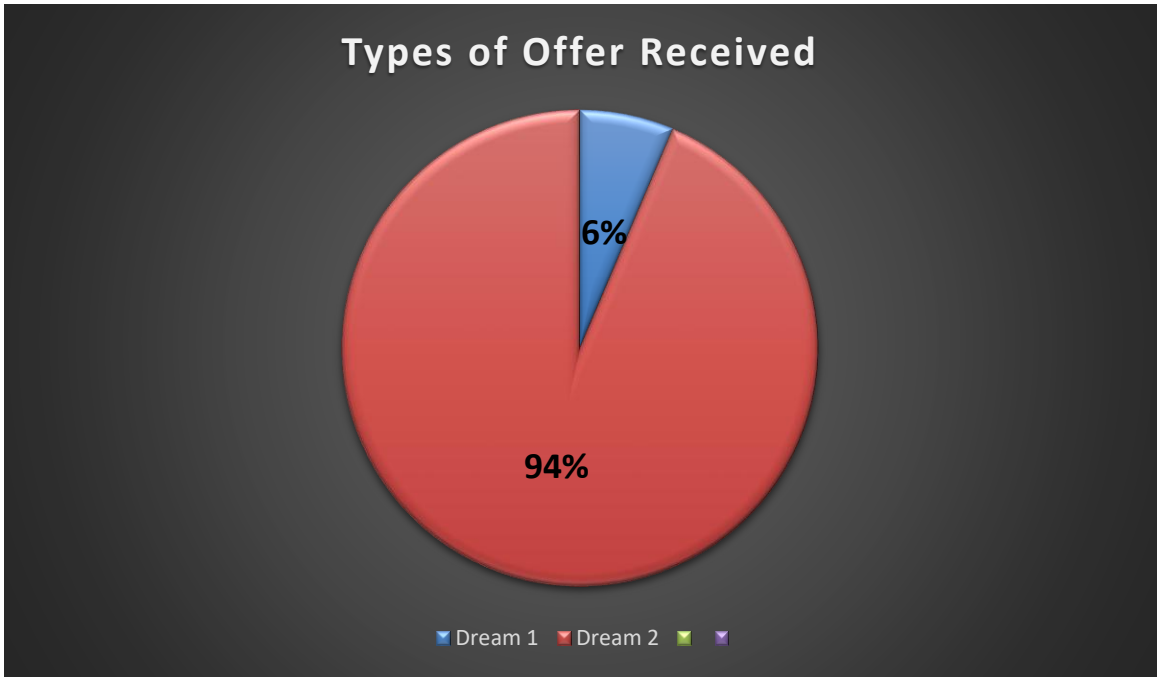
Academic Year : 2024-25

Sr. no.	Semester	Total no of students appeared	Total no of students passed	% of passing in the subject
1	III	203	193	95.07
2	IV	203	190	93.60
3	V	206	198	96.12
4	VI	206	201	97.57
5	VII	100	100	100
6	VIII	100	100	100

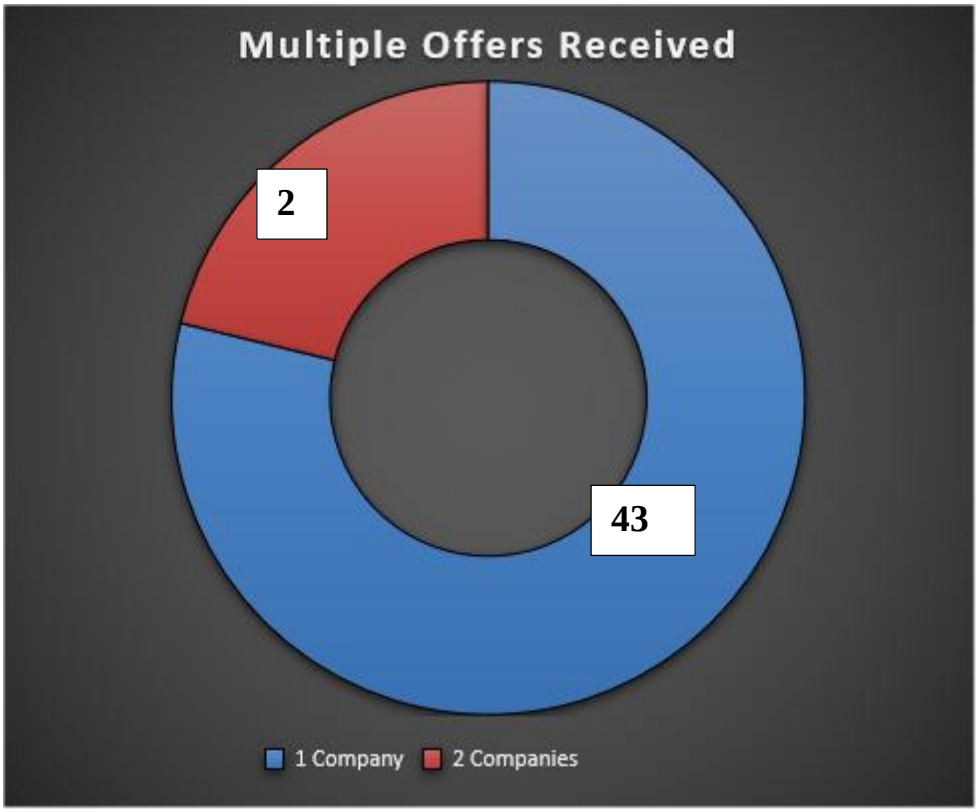
7 PLACEMENT DATA

Total no. of Students Placed Company Wise = 47 (Including Multiple Placement Offers)

Sr. No.	Company Name	Salary Per Annum(LPA)	No. of Students Placed
1.	ZS Associates	13.65	02
2.	Here Technology	12	1
3.	Sure Financial	10	1
4.	Jaro	10	1
5.	Indus Valley Partner	8.52	1
6.	Tresvista	8.4	1
7.	Godrej	7.84	2
8.	Zeus Learning	7.1	1
9.	Fractal Analytics	7	1
10.	Delloite	6.7	3
11	GEP	6.5	3
12.	EY	6.48	2
13.	Frootle	6	4
14.	KPMG	6	2
15.	Gandhi Automation	4.6	2
16.	Capgemini	4.25	19
17.	Pagazo	4	1
Minimum CTC in LPA: 4.0 LPA		**Maximum CTC in LPA: 13.65 LPA**	



Super Dream: > 20 LPA , Dream 1: > 12 LPA and less than 20 LPA, Dream 2 : 4 LPA and less than 12 LPA, Normal / Mass : < 4 LPA



ACADEMIC BULLETIN

Period: 1st January 2026 – 30th June 2026

1 ABOUT DEPARTMENT

1.1 Department Information

- Started in the year 1999 with the intake of 30 and which was increased to 60 in the subsequentyear.
- The intake was increased to 120 in the Academic Year 2010 – 11.
- In the Academic Year 2011 – 12, Department has started M.E. Program in Electronics & telecommunication with an intake of 18 students.
- For the first time Department got NBA accreditation for two years from January 2013. In second Outcome based evaluation, Department got NBA accreditation for three years from July 2017.
- The Department started with Ph.D. program in Academic Year 2015 – 16 with an intake of 10 students.
- The department is having highly qualified, experienced and dedicated faculties and supporting staff.
- Well-equipped labs and fully air-conditioned classrooms with projectors.
- The intake was increased to 180 in the Academic Year 2022 – 23.

1.2 Vision of the Department

To develop technically competent and socially responsible Electronics and Telecommunication engineers capable of fulfilling expectations at indigenous and global levels.

1.3 Mission of the Department

- To provide a conducive educational environment for students by providing goodinfrastructural facilities, knowledge base and excellent faculty support.
- To provide a strong foundation of core knowledge and exposure to research culture.
- To motivate learners to acquire adequate professional and soft skills, to develop personalitytraits and eventually transform them as life-long learners.
- To strive and achieve practical exposure by maintaining good rapport with industry and professional network.

1.4 Program Educational Objectives (PEOs)

- **PEO1:** To prepare learners for graduate studies by providing strong foundation of basic sciences, computer programing and thus, develop analytical aptitude, and problem-solving abilities.
- **PEO2:** To develop a fundamental understanding of electronic & integrated circuits, communication systems and allied disciplines.
- **PEO3:** To develop core competency and expertise in the diverse areas of communication covering Signal processing, Electromagnetic Engineering, Embedded Systems, ComputerCommunication and Advanced Wireless Networks domains.
- **PEO4:** To inculcate competencies and aptitude in extending acquired technical knowledge to solve real life issues with high professional and ethical standards.
- **PEO5:** To develop proficiency in soft skills and deliver adequate personality traits to enablethe pass outs to pursue higher education, to find competitive employment opportunities and/or pursue entrepreneurial ventures.

1.5 Program Specific Outcomes (PSOs)

- Design and implement electronic systems that perform analog and digital signal processing functions as applied in embedded systems, multimedia processing and VLSI design.
- Design and implement necessary components (circuits, antennas, microwave devices) of modern RF/Wired/Wireless communication systems.
- Cultivate necessary soft skills, aptitude and programming skills to solve real-world problems.

2. ADMINISTRATION

IETE COMMITTEE

Prof. Amit Deshmukh — Dr. Anuja Odhekar

PROJECT COORDINATOR

Prof. Amit Deshmukh — Dr. Ameya Kadam

DEPARTMENTAL LIBRARY

Prof. Amit Deshmukh — Prof. Archana Chaudhari

ALUMNI COMMITTEE

Prof. Amit Deshmukh — Prof. Ranjushree Pal

NBA CORE COMMITTEE

Prof. Amit Deshmukh — Dr. V. V. Kelkar (PC)

Dr. Ameya Kadam (PC)

AUTONOMY COMMITTEE

Dr. Poonam Kadam — Prof. Shreeja Nair

TIME-TABLE COMMITTEE

Prof. Archana Chaudhary — Prof. Mrunalini Pimpale

Prof. Tushar Sawant

PLACEMENT COORDINATOR

Dr. Aarti Ambekar — Dr. Supriya Dicholkar

Prof. Tushar Sawant

NPTEL and IBM COORDINATOR

Dr. V. V. Kelkar

3. IETE- SF

The Electronics and Telecommunication Department of Dwarkadas. J. Sanghvi College of Engineering presents Institution of Electronics and Telecommunication Engineers- Student Forum (IETE-SF). The student chapter with a working force committee of 22, consisting of second year and third year students, hosted a few of the most quintessential and technically challenging events. A membership drive was conducted at the start of the year with an overwhelming response. (www.djsceietesf.com)

IETE Organizing Committee Structure

IETE SF Branch Counsellor: - Dr. Anuja Odhekar

Chairman	Anmol Parekh
Vice-Chairperson	Krish Tawde
Secretary	Jiya Mevada
Treasurer	Ahaan Deshpande
DJ-Strike Coordinator	Om Kulkarni Payal Vaishnav

Head Of Departments:	
Publicity	Rudra Nisar Advait Sawant
Marketing	Krishna Misra Tanvi Mehta
Technical	Shubham Tayade Abbas Damaniya
Infotech	Aditya Ralhan Agrim Tawani
Creatives	Jyotiraditya Bhat
Events	Aryan Bhalkar, Prayag Kartha
Editorial	Akanshka Raina, Garima Singh
Book Bank	Om Kulkarni
Component Bank	Om Kulkarni

4. DEPARTMENT ACTIVITIES

4.1 Value Added Program under IETE-SF

Book Bank

IETE-SF provides the students with a book bank facility where they can issue reference books at nominal rates for the entire semester. Students who want a better insight into the subject avail this facility as these reference books aid in developing a good understanding of the topics and enable them to consolidate their foundation of the subject. Book bank has more than 60 book titles as per the syllabus requirement for 3rd to 8th semester. This activity not only motivates students to use reference books prescribed in syllabus but also explore them in the library management system. The alumni who worked as "Book-Bank" coordinators received paid assistance-ship in the library during their master program.

Component Bank

IETE-SF provides a component bank facility where students can borrow electronic components which they require for executing multiple projects both in and outside of the curriculum. They can utilize the facility by initially paying 50% of the cost and getting a refund of 20% on returning the components, provided that they are undamaged.

4.2 Hands on workshop on VLSI and FPGA Design

- Date- - 22nd Feb 2026
- Venue- EXTC Labs, 5th floor.
- Time- 8:30 am – 6.00 pm
- No. Of Participants: 40 (UG Engineering Students Across Mumbai)
- Organised By: DJS MicroMinds (VLSI Club)
- Resource Person: Dr. Poonam Kadam

OBJECTIVE:

- To provide a foundational understanding of VLSI technology, including the integration of transistors into single chips for high-speed and low-power systems.
- To establish a clear comparative understanding of ASIC and FPGA design methodologies, highlighting when to prioritize flexibility versus performance.
- To equip participants with practical Verilog fundamentals, enabling them to describe and simulate digital hardware through various modeling techniques.
- To bridge academic theory with practical application by synthesizing Verilog code into physical hardware using the Basys 3 FPGA development board.

CONTENT:

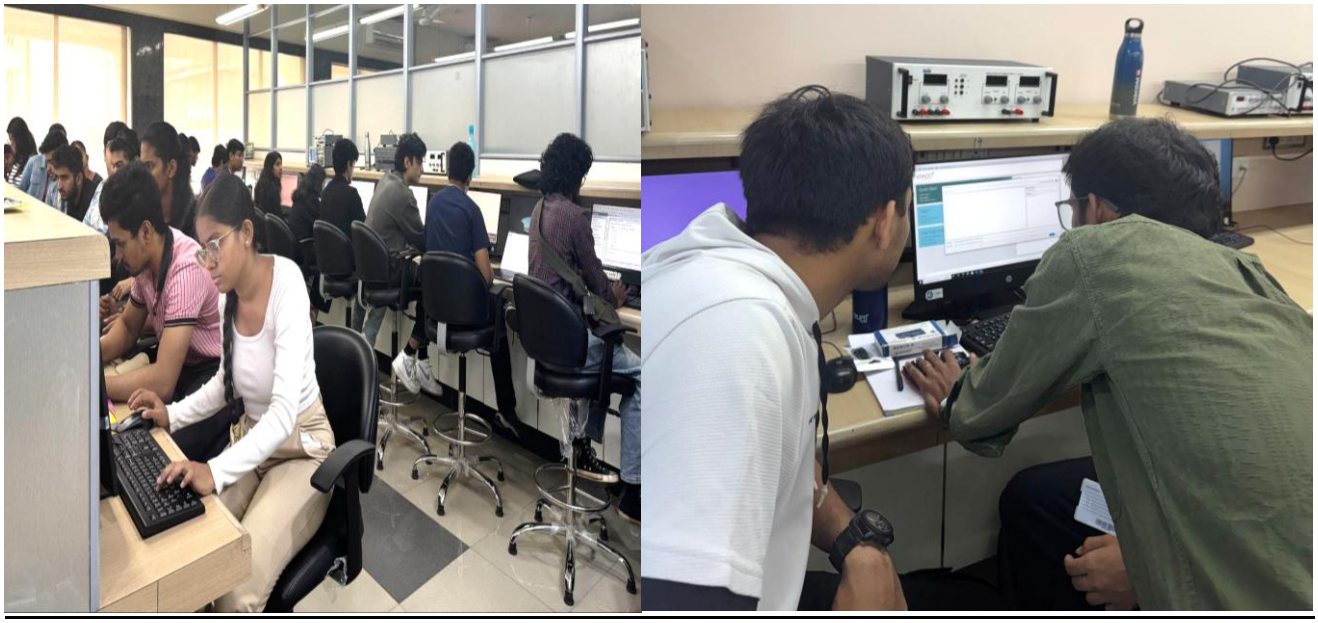
On 22nd February, the DJS MicroMinds (VLSI Club) committee of Dwarkadas J. Sanghvi College of Engineering (DJSCE) organized a Hands-on FPGA Workshop. The event was aimed at introducing students to the core concepts of VLSI design and hardware description, guided by Dr. Poonam Amol Kadam, Associate Professor in EXTC Department and the faculty In charge of DJS MicroMinds VLSI Club. The session transitioned students from theoretical digital logic to practical RTL design and hardware implementation.

EVENT PROCEEDINGS:

The session commenced with Dr. Poonam Kadam introducing the vast landscape of VLSI, highlighting growing industry opportunities across Front End Design, Physical Design, and Verification. A detailed comparison was drawn between the high performance of ASICs and the flexible, reprogrammable nature of FPGAs. Students also explored internal FPGA architecture. Dr. Poonam Kadam introduced Verilog hardware description language, covering Structural, Dataflow, and Behavioral modeling. Participants learned critical coding practices and simulated digital building blocks, including multiplexers and full adders. The workshop culminated with practical synthesis on the Basys 3 FPGA board. Students successfully implemented the full adder designs and a decade counter, utilizing a clock divider and 7-segment decoder to visually display outputs directly on the board's hardware.

Throughout the session, students actively clarified their doubts regarding the digital design flow. The hands-on experience allowed the students to practically apply the concepts and debug their errors along with the volunteers and the teacher. Students also inquired about the types of projects they can work on to apply the concepts they learnt through the workshop. As students moved to hardware synthesis, they asked about the purpose of the XDC (.xdc) file and how to make one.

EVENT PICTURES:



ACKNOWLEDGEMENTS:

The success of the Hands-on VLSI and FPGA Design Workshop was made possible through the dedicated efforts of the DJS MicroMinds team and the unwavering support of our respected Principal, who provided the platform to conduct this advanced technology session.

We would also like to express our appreciation to Dr. Amit Deshmukh, Professor and Head of the EXTC Department, for facilitating the necessary resources to successfully conduct this highly technical session.
We are deeply grateful to Dr. Hari Vasudevan, Principal, for his constant encouragement, visionary leadership, and for fostering an academic environment that promotes technical excellence and innovation.

OUTCOME:

The workshop successfully bridged the gap between theoretical digital electronics and physical hardware prototyping. By writing Verilog and generating bitstreams, students gained practical exposure to the FPGA Design Flow, from design entry to implementation. Working directly with the Xilinx Artix-7 FPGA on the Basys 3 boards demystified hardware synthesis and enhanced the participants' debugging skills. The comprehensive overview of industry methodologies sparked a deepened technical curiosity, motivating students to explore advanced RTL design and pursue further projects in semiconductor technology.

Dr. Poonam A Kadam
Associate Professor, EXTC Dept.
Faculty In-charge, DJS MicroMinds,
DJSCE, Mumbai

Dr. Hari Vasudevan
Principal,
DJSCE, Mumbai

4.3 Dr. P.B. Parikh Endowment Lecture

- Date- - 2nd March 2026
- Venue- Seminar Hall, 3rd Floor
- Time- 2:30 – 4 pm

OBJECTIVE:

- To provide students with a deeper understanding of microcontroller applications and clarity about practical challenges in embedded systems.
- To emphasize that error handling is in the hands of engineers, who must ensure MCU responsiveness for robust systems.
- To enhance technical knowledge, troubleshooting and problem-solving skills, and industry readiness among students.

CONTENT:

On 2nd March 2026, the IETE Students' Forum and the Department of Electronics and Telecommunication Engineering (EXTC) of Dwarkadas J. Sanghvi College of Engineering (DJSCE), successfully hosted the Dr. P.B. Parikh Endowment Lecture, in collaboration with IETE Mumbai Centre. The session was delivered by Mr. Manoj Bhataria, CTO, Devlata Technologies Pvt. Ltd., who shed light upon the importance of microcontroller responsiveness in modern embedded systems, guiding students with his expertise and experience in this field.

The lecture exposed students to obstacles encountered in practical embedded systems, emphasising that faults in systems are never random, but always due to architectural flaws. Microcontroller systems in reality often experience interference, timing uncertainty and unexpected resets, all of which must be contained through fault-tolerant and resilient system design.

Students were made aware of ghost resets that occur in the microcontroller, often due to unstable voltages, EM interference, etc. Fluctuating power plays a major role in system mishaps, causing the MCU to jump instructions, corrupt flags or execute in an endless loop. To make the system robust, brown-out resets and watchdogs were some suggested methods for protection and recovery of firmware.

The microcontroller also waits at one line of a program until a certain condition is satisfied. Power failure, sensor failure or bus hangs can trigger this "blocking", making the system unresponsive. SCL bus hangs due to interference are caused by spikes that imitate clock signals, confusing the MCU. In practical applications like weather stations, sensor data may remain constant for a long period of time, and despite functioning correctly, the MCU assumes a fault and exits the loop.

The speaker thus suggested effective methods to avoid sudden errors. Students understood the necessity of external supervisors, interrupt management, error handling codes and frequent progress reports. Machine failure is silent, but always due to architectural flaws. Engineering responsiveness is a professional responsibility.

The session elucidated the hidden challenges faced by real-world microcontrollers, and how they can be overcome by understanding working principles, identifying errors and engineering responsiveness.

EVENT PROCEEDINGS:

The programme commenced with a warm welcome extended to all dignitaries, faculty members, and students present for the Dr. P. B. Parikh Endowment Lecture 2026, organized by the IETE Students' Forum in collaboration

with the Department of Electronics and Telecommunication Engineering, DJSCE, and IETE Mumbai Centre.

The session began with an introduction to the significance of the Dr. P. B. Parikh Endowment Lecture, highlighting his invaluable contributions to the field of technical education and his vision of fostering innovation and excellence among engineering students.

This was followed by the ceremonial lighting of the lamp, performed by esteemed dignitaries including Dr. Shivaji Ghungrad, Dr. Vikas Gupta, Dr. Hari Vasudevan, Mr. Kartik Parikh, Dr. Narendra Shekokar, and Prof. Amit A. Deshmukh, accompanied by a Saraswati Vandana, symbolizing the invocation of knowledge and wisdom.

Subsequently, Dr. Hari Vasudevan, Principal of DJSCE, addressed the gathering, sharing his insights on the importance of technical competence, innovation, and industry-academia collaboration. His address set an encouraging tone for the session. The dignitaries were then felicitated in recognition of their presence and contributions.

Following this, Dr. Shivaji Ghungrad, Chairman of IETE Mumbai Centre, delivered an insightful address emphasizing the role of professional bodies like IETE in shaping future engineers and promoting continuous learning.

The Guest of Honour, Mr. Kartik Parikh, CEO of Fastech Telecommunications, then addressed the audience. Drawing from his extensive experience in the telecommunications industry, he spoke about the importance of addressing engineering challenges at the foundational level and emphasized the need for strong problem-solving skills in ensuring system reliability and responsiveness.

The highlight of the session was the Endowment Lecture delivered by Mr. Manoj Bhataria, Chief Technology Officer at Devlata Technologies Pvt. Ltd., on the topic “Ensuring MCU Responsiveness.” He began by providing a practical perspective on microcontroller architecture and elaborated on the various challenges encountered in real-world embedded systems.

He explained how system failures are often the result of architectural issues rather than random faults, and discussed the impact of power instability, electromagnetic interference (EMI), and timing uncertainties on system performance. He further elaborated on how microcontrollers can experience issues such as ghost resets, instruction jumps, corrupted flags, and infinite loops due to such disturbances.

Mr. Bhataria highlighted the problem of blocking conditions in programs, where the microcontroller remains stuck waiting for a condition to be satisfied, often caused by sensor failures, communication errors, or bus hangs. He illustrated how such situations can lead to complete system unresponsiveness if not handled properly.

To address these challenges, he shared several practical techniques to improve system robustness, including the use of watchdog timers, brown-out reset mechanisms, external supervisors, effective interrupt handling, structured error-handling codes, and continuous system validation. He emphasized that reliable system design requires proactive fault detection and recovery mechanisms.

He concluded the lecture by reinforcing that machine failures are often silent but rooted in design flaws, and that ensuring microcontroller responsiveness is a critical responsibility of engineers.

The session concluded with a Vote of Thanks delivered by Dr. Amit A. Deshmukh, Head of the EXTC Department, expressing gratitude to all dignitaries, speakers, organizers, and participants for their valuable contributions. The programme ended with the National Anthem, followed by refreshments for all attendees.

EVENT PICTURES:

ACKNOWLEDGEMENTS:

The successful organization of the Dr. P. B. Parikh Endowment Lecture 2026 was made possible through the collective efforts and dedication of the faculty members and organizing team of the Department of Electronics and Telecommunication Engineering.

We extend our sincere gratitude to **Dr. Anuja A. Odhekar, Associate Professor and Branch Counsellor of IETE-ISF**, for her constant guidance, encouragement, and unwavering support in planning and executing this event seamlessly.

We express our heartfelt appreciation to **Mr. Manoj Bhataria, Chief Technology Officer at Devlata Technologies Pvt. Ltd.**, for delivering an insightful and highly engaging lecture. His practical approach and depth of knowledge in embedded systems and microcontroller technologies provided students with valuable real-world perspectives.

We would also like to specially acknowledge **Mr. Kartik Parikh, CEO of Fastech Telecommunications and son of Dr. P. B. Parikh**, for gracing the occasion as the Guest of Honour. His presence added great significance to the event, and his address offered meaningful insights while honouring the legacy and vision of Dr. P. B. Parikh.

Our sincere thanks to **Dr. Amit A. Deshmukh, Professor and Head of the Department of Electronics and Telecommunication Engineering**, for his continuous encouragement and for providing a platform to conduct such an enriching and impactful technical session.
We also extend our gratitude to all dignitaries from IETE Mumbai Centre for their esteemed presence and support, which greatly contributed to the success of the event.

Finally, we thank all the participating students for their enthusiastic involvement and active engagement, which made the session interactive and truly successful.

IMPACT:

The enriching lecture on microcontroller responsiveness provided students with valuable exposure to the hidden problems behind embedded systems. The session strengthened their understanding of microcontroller structure and how to tackle architectural faults.

Students gained clarity on the role of microcontrollers in real-world applications, understanding the necessity of fault detection and responsible fault containment. They learnt about multiple methods through which errors can be handled, and how progress can be frequently validated.

Overall, the session successfully bridged the gap between classroom learning and practical industrial functionality, inspiring students to pursue innovation and technical excellence with clarity in the field of embedded systems.

4.4 Expert talk on AI Trends and Applications

- Date- 11th March 2026
- Venue- Seminar Hall, 3rd floor, DJSCE
- Time- 08:00 am- 10:00 pm

OBJECTIVE:

The Expert Talk was organized to:

- Collaborate current syllabus of Artificial Intelligence with it's applications in Industry for giving insights about current trends in Agentic AI.
- Provide help to current students for getting opportunity to work on live projects in AI and make them ready with skillsets required for the same.

CONTENT:

The Department of Electronics and Telecommunication Engineering (EXTC) of Dwarkadas J. Sanghvi College of Engineering organized an Expert Talk on **"AI Trends and Applications"** on **11 March 2026** in the **Seminar Hall, 3rd Floor, DJSCE**, from **8:00 AM to 10:00 PM**. The session was conducted to familiarize students and faculty members with the latest advancements in Artificial Intelligence and its growing impact across various industries.

The expert talk witnessed enthusiastic participation from undergraduate students, faculty members, and AI enthusiasts. The session aimed to provide participants with a comprehensive understanding of emerging AI technologies, current industry trends, and the practical applications of Artificial Intelligence in solving real-world problems.

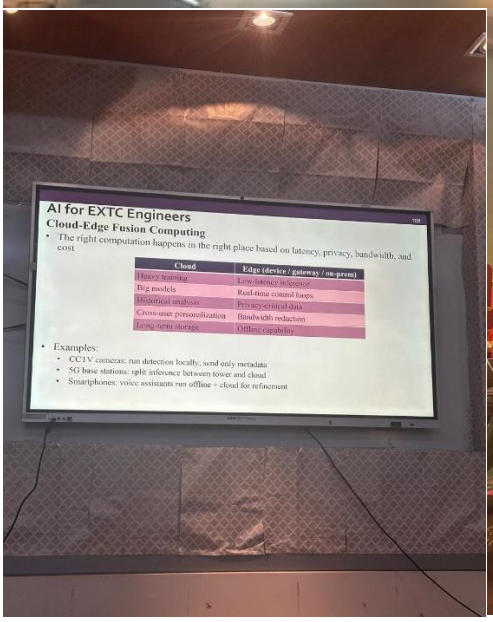
The speaker discussed recent developments in machine learning, deep learning, generative AI, natural language processing, computer vision, and intelligent automation. The session highlighted the transformative role of AI in sectors such as healthcare, finance, manufacturing, education, cybersecurity, and smart cities, while emphasizing the importance of ethical AI practices, responsible innovation, and data privacy.

The expert also shared valuable insights into the skills required for building a successful career in Artificial Intelligence, the importance of continuous learning, and the growing demand for AI professionals in academia, research, and industry. Participants were introduced to current AI tools, emerging technologies, and future opportunities in the field.

An interactive question-and-answer session followed the talk, during which students actively engaged with the speaker by discussing AI applications, research opportunities, career prospects, and industry expectations. The expert addressed the participants' queries and encouraged them to undertake innovative projects and interdisciplinary research in Artificial Intelligence.

The expert talk concluded with a vote of thanks, acknowledging the speaker's valuable contribution and the enthusiastic participation of the attendees. Overall, the session was highly informative and enriching, enhancing participants' understanding of AI trends and applications while motivating them to explore emerging technologies and prepare for the rapidly evolving digital landscape.

Event Pictures:



Dr. Supriya Dicholkar, Prof. Abhilasha Raghatate
Al ML Honor faculty SE

Prof Amit A. Deshmukh
Prof & Head EXTC department

4.5 Alumni Meet

- Date- 14th March 2026
- Venue- Seminar Hall, 1st floor, DJSCE
- Time- 10:00 am- 03:00 pm

OBJECTIVE:

The seminar was organized to:

- Collaborate current students with Alumni for giving insights about current trends in Industry
- Provide help to current students for getting Internship and jobs in Industries.

CONTENT:

The Department of **Electronics and Telecommunication Engineering (EXTC)** of Dwarkadas J. Sanghvi College of Engineering organized an **Alumni Meet on 14 March 2026 from 10 am to 3 pm**. The meet was in hybrid mode where alumni from abroad joined online and from India joined offline. The event aimed to strengthen the connection between the department and its alumni while encouraging collaboration for student development and industry interaction.

Around **35 alumni** from different graduating batches attended the meet. The event provided an opportunity for alumni to reconnect with their alma mater, interact with faculty members, and share their professional experiences with the department.

The **Head of the Department (HOD), Prof. Amit A Deshmukh** addressed the gathering and spoke about the **importance of industry exposure for students**, particularly highlighting the **On-the-Job Training (OJT)** initiative under the new academic framework. The HOD explained how OJT helps students gain practical experience, develop industry-relevant skills, and better prepare for professional careers.

During the discussion, alumni were encouraged to **support the department by offering internship and training opportunities** for students. The alumni appreciated the initiative and expressed their willingness to stay connected with the department and contribute to student development.

The meet concluded with an **interactive session**, where alumni shared their insights, career journeys, and suggestions for strengthening industry–academia collaboration.

Overall, the alumni meet was a **productive and engaging event**, reinforcing the strong bond between the department and its alumni while opening avenues for future collaboration.

Event Pictures:

Ranjushree Pal
Alumni Co-ordinator

Prof Amit A. Deshmukh
Prof & Head EXTC department

4.6 DJS Strike

- Date- 16th March 2026
- Venue- EXTC Laboratories (RF, SPL, EDL, PL, ESL, BCEL Labs) DJSCE.
- Time- 09:00 am- 01:00 pm

OBJECTIVE:

The seminar was organized to:

- To provide a platform for students to present their **Innovative Product Development (IPD)** group projects.
- To encourage innovation, technical thinking, and practical implementation of engineering concepts.
- To evaluate students based on their project design, execution, and presentation skills.
- To shortlist the best projects for the national-level competition **DJS Spark 2026.**

CONTENT:

On 16th March 2026, the Department of Electronics and Telecommunication Engineering of Dwarkadas J. Sanghvi College of Engineering successfully organized DJS Strike, an annual technical event cantered around student-led IPD projects. The event brought together students from various groups who showcased their innovative ideas and working prototypes across diverse domains such as healthcare, agriculture, automation, and communication systems.

A total of 54 teams participated in the competition, with presentations conducted across six different laboratories—RF Lab, SPL Lab, EDL Lab, PL Lab, ESL Lab, and BCEL Lab. Each lab functioned as an independent evaluation centre, ensuring smooth execution and effective time management throughout the event.

The event commenced with an inaugural ceremony led by the Principal, Dr. Hari Vasudevan, along with the Vice Principal and respected faculty members. The inauguration highlighted the importance of innovation in engineering education and encouraged students to actively engage in problem-solving and research-driven development.

EVENT PROCEEDINGS:

The event was systematically organized into two rounds to ensure a fair and comprehensive evaluation of all participating teams.

Round 1: Initial Evaluation

The first round of the competition began at 9:00 a.m., where all 54 teams presented their projects in their respective laboratories as per the scheduled timetable. Each team was allotted 10 minutes to present their project, which included explaining the problem statement, methodology, working prototype, and potential real-world applications.

The evaluation panels in each lab consisted of faculty members and experts who assessed the projects based on multiple criteria such as innovation, technical complexity, feasibility, design approach, and clarity of presentation. The students demonstrated a wide range of ideas, from socially impactful solutions

like healthcare monitoring systems to technologically advanced applications such as drones and smart devices.
The atmosphere during this round was highly dynamic and competitive, with multiple presentations occurring simultaneously across labs. Students actively engaged with the judges, answered questions, and justified their design decisions. This round not only tested the technical knowledge of the participants but also their confidence, clarity, and ability to communicate their ideas effectively.
At the end of Round 1, a total of 3 teams from each lab were shortlisted based on their performance, resulting in 18 teams advancing to the next round.

Round 2: Final Evaluation
The second round consisted of the shortlisted 18 teams who presented their projects again before a more focused evaluation panel. In this round, greater emphasis was placed on the depth of the project, practical implementation, scalability, and innovation.
The shortlisted teams were expected to provide more detailed explanations of their system design, demonstrate the working of their prototypes more effectively, and address advanced technical questions posed by the judges. This round allowed judges to distinguish between good ideas and truly exceptional projects with strong real-world applicability.
The competition in this stage was intense, as all teams had already cleared the initial screening and displayed high levels of technical competence. The judges carefully evaluated each project before finalizing the top-performing teams.

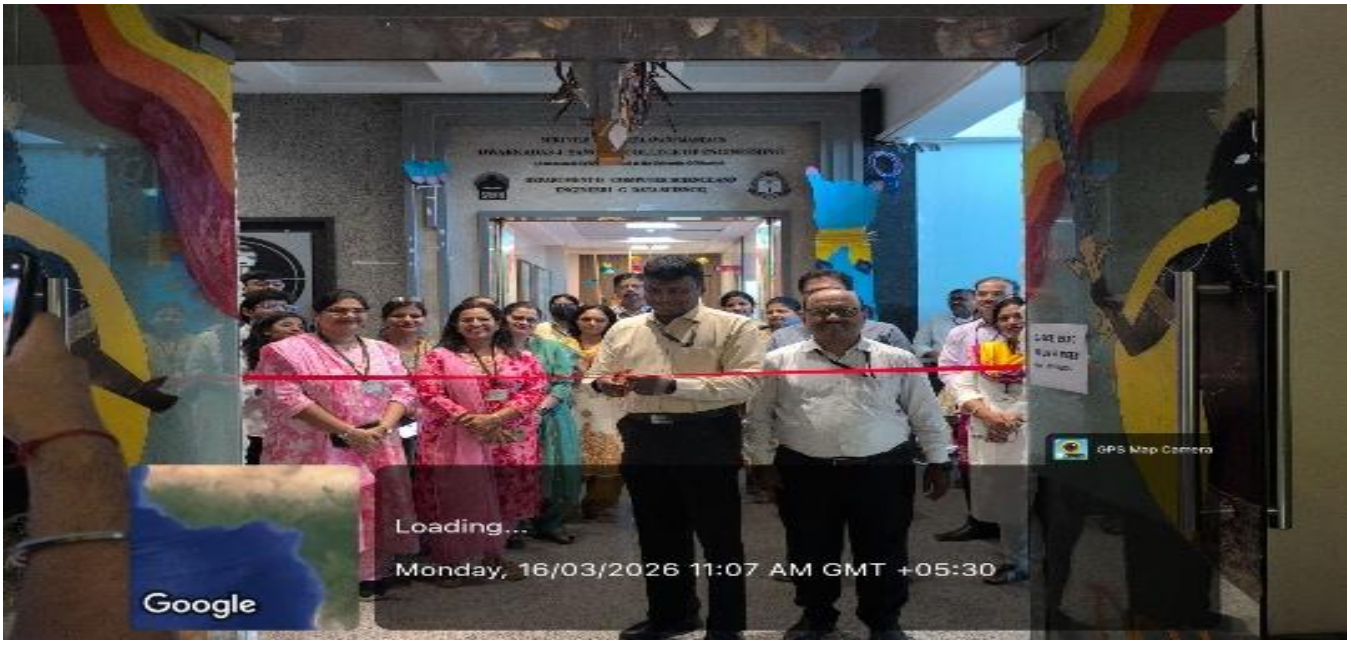
Final Selection and Announcement
Based on the cumulative performance across both rounds, the top teams were selected as winners. These teams demonstrated outstanding innovation, technical execution, and presentation skills. The results were officially announced at the end of the event, recognizing the efforts of the participants and celebrating their achievements.
The selected teams were given the opportunity to represent the college at the national-level competition, DJS Spark 2026, marking a significant milestone in their academic journey.

RESULTS / WINNERS:

The following teams were selected as top performers and promoted to DJS Spark 2026:

- **Group 33** – Coal Mine PPE Detection Kit
- **Group 31 (SE)** – Kanda Crate
- **Group 26** – Drone for Agriculture Surveillance
- **Group 44** – "DRISHTI" – A Braille Printer
- **Group 37** – Smart Stethoscope and Contactless Vital Signs Monitor
- **Group 5** – Broadband Antenna

Event Pictures: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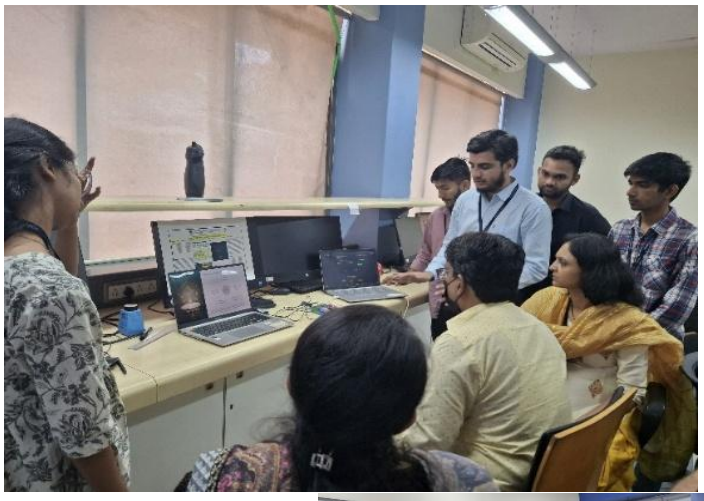

4.7 GMRT Industrial Visit

- **Date-** 27th March 2026
- **Venue-** GMRT, Ozar, Maharashtra
- **Time-** 6:00 AM – 11:00 PM

OBJECTIVE:

- To provide students with practical exposure to advanced radio astronomy systems and technologies at GMRT.
- To bridge the gap between theoretical knowledge and real-world engineering applications.
- To understand the working principles of large-scale antenna arrays and signal processing techniques.
- To encourage curiosity and interest in interdisciplinary domains combining electronics, communication, and astrophysics.

CONTENT:

On 27th March 2026, the Department of Electronics and Telecommunication Engineering of Dwarkadas J. Sanghvi College of Engineering organized an industrial visit to the Giant Metrewave Radio Telescope (GMRT), located in Ozar, Maharashtra. The visit aimed to provide students with firsthand exposure to one of the world's leading radio astronomy observatories.

The journey commenced early in the morning, with students and faculty departing from Vile Parle Station at 6:00 AM. Upon arrival at GMRT, the group was welcomed by the technical staff, who provided an introductory session on the facility, its history, and its significance in the field of radio astronomy. Students were introduced to the fundamentals of radio telescopes, including their design, working principles, and applications in studying celestial phenomena.
The visit included guided tours of the antenna array and control facilities, where students observed the large parabolic dish antennas and gained insights into their alignment, signal reception, and data processing mechanisms. The experts at GMRT explained how multiple antennas work together as an array to capture high-resolution signals from distant astronomical sources.

An interactive session was also conducted, allowing students to engage with researchers and clarify their doubts regarding instrumentation, signal processing, and ongoing research projects. This interaction helped students understand the interdisciplinary nature of the field, combining electronics, communication, and astrophysics.

The visit concluded in the evening, with students returning to Vile Parle Station by 11:30 PM, enriched with practical knowledge and a deeper appreciation of large-scale scientific systems.

EVENT PROCEEDINGS:

The industrial visit was carefully planned and executed to ensure a structured and informative experience for all participants.

The journey commenced at 6:00 AM, with students and faculty assembling at Vile Parle Station and departing for GMRT by bus. The travel arrangements were well-coordinated, ensuring a comfortable and timely arrival at the site. En route, the group made a halt at Ozar for lunch, allowing participants to rest and refresh before proceeding to the facility.

Upon reaching the facility, the participants were received by the GMRT staff and directed to an orientation session. This session provided an overview of the Giant Metrewave Radio Telescope, its historical significance, and its contributions to the field of radio astronomy. The experts introduced students to the fundamentals of radio wave detection and the role of large antenna arrays in observing celestial objects.

Following the introductory briefing, students were taken on a guided tour of the GMRT premises. They visited the antenna array fields, where they observed the massive parabolic dish antennas and learned about their structural design, positioning, and synchronization. The functioning of the central control system and signal processing units was also explained, highlighting how data collected from multiple antennas is combined and analyzed.

An interactive session was conducted during the visit, allowing students to engage directly with scientists and technical staff. Students actively participated by asking questions related to instrumentation, signal transmission, noise reduction techniques, and ongoing research activities at GMRT. This interaction enhanced their understanding of real-world engineering challenges and research practices.

The visit was conducted in an organized and disciplined manner, with students adhering to the guidelines provided by the facility. Faculty members ensured smooth coordination throughout the visit, maintaining safety and time management.

After concluding the visit, the group began the return journey, with a scheduled stop at Khopoli Food Plaza for dinner, and reached Vile Parle Station by 11:30 PM, marking the successful conclusion of the industrial visit.

EVENT PICTURES:

ACKNOWLEDGEMENTS:

The successful organization of the GMRT industrial visit was made possible through the collective efforts of the faculty coordinators, support staff, and student volunteers. The department expresses its sincere gratitude to the faculty members for their guidance and supervision throughout the visit. We also extend our thanks to the institute authorities for their support in facilitating this educational initiative.

Special appreciation is extended to the team at GMRT for their cooperation, insightful guidance, and for providing students with an enriching learning experience. Their efforts in conducting informative sessions and guided tours were highly valuable.

IMPACT:

The industrial visit to GMRT provided students with significant practical exposure to advanced technologies in the field of radio astronomy. It enhanced their understanding of large-scale engineering systems and their real-world applications.

The visit helped bridge the gap between theoretical concepts and practical implementation, allowing students to visualize how principles of electronics and communication are applied in research environments. It also sparked curiosity and interest in interdisciplinary domains, encouraging students to explore opportunities in research and innovation.

Overall, the experience contributed to broadening students' technical perspective and inspired them to engage more deeply with emerging technologies and scientific advancements.

Dr. Anuja A Odhekar
Associate Professor,
Branch Counsellor,
IETE-ISF, DJSCE, Mumbai

Prof. Amit A. Deshmukh
Prof. & Head, Department of
Electronics and Telecommunications
Engineering, DJSCE, Mumbai

4.8 UNPLUGGED 3.0: ENTER THE WILD

Date: 11th April 2026 and 12th April 2026
Venue: DJSCE Campus
Time: 9:00 a.m. (Saturday) – 6:00 p.m. (Sunday)

OBJECTIVE

To cultivate innovation, rapid prototyping, and practical hardware design skills within a high-pressure 24-hour environment, while addressing real-world challenges in wildlife conservation. The hackathon aimed to push participants beyond theoretical understanding, encouraging them to design, build, and iterate under constraints similar to real engineering environments. It focused on developing technical resilience, problem-solving under time pressure, and the ability to translate conceptual ideas into functional hardware systems with tangible impact.

INTRODUCTION

Unplugged returned for its third edition with a sharper, more immersive focus—where innovation met endurance. *Unplugged 3.0: Enter the Wild* was designed not merely as a competition, but as an experience that tested both technical capability and mental persistence.

With the theme **"Wildlife Conservation - Jurassic World,"** this year's edition reframed engineering challenges through an ecological lens, placing participants in a scenario where technology serves as a tool for preservation rather than just performance. The hackathon created an environment that demanded quick thinking, adaptability, and sustained effort, simulating real-world engineering conditions where solutions must evolve continuously under pressure.

Over the course of 24 hours, participants engaged in an intense cycle of ideation, prototyping, testing, and refinement—each iteration bringing them closer to building systems that were not only functional but also contextually relevant.

CONTENT & THEME

Domain: Smart Wildlife Systems

Jungle safaris are structured eco-tourism initiatives within protected reserves, designed to balance conservation efforts with controlled public access. However, the management of such systems remains largely fragmented and manual, leading to inefficiencies in tracking wildlife movement, regulating tourist distribution, and maintaining ecological balance across zones.

A lack of real-time monitoring and integrated data systems often prevents forest authorities from making informed decisions, leading to overcrowding in popular areas, underutilization of other zones, and increased stress on wildlife habitats. As eco-tourism continues to grow, the need for intelligent, data-driven infrastructure becomes increasingly critical.

Unplugged 3.0 addressed this gap by introducing the concept of a smart safari ecosystem. Participants were challenged to design solutions that could seamlessly integrate sensing, tracking, and decision-making systems to improve operational efficiency while preserving ecological integrity.

The expected solutions focused on:

- Real-time tracking of wildlife and environmental conditions
- Monitoring and optimising tourist movement across safari zones
- Reducing manual dependency through automation and structured data systems
- Enhancing sustainability by minimizing ecological disruption

By anchoring the challenge in a real-world conservation problem, the hackathon encouraged participants to move beyond isolated hardware components and think in terms of scalable, system-level solutions.

EVENT PROCEEDINGS

Inauguration Ceremony (11th April 2026 – Saturday Morning)

Unplugged 3.0 commenced on the morning of 11th April 2026 at 7:30 a.m. with the traditional lighting of the lamp in the presence of the Principal, Dr. Hari Vasudevan, the Vice Principal, Dr. Narendra Shekokar, and the Head of the Department, Dr. Amit Deshmukh. The inauguration marked the formal beginning of the 24-hour hardware hackathon and set the tone for a highly competitive and innovation-driven event focused on embedded systems, IoT, and intelligent automation.

The speakers highlighted the importance of interdisciplinary engineering, real-world problem solving, and collaborative innovation, encouraging participants to build solutions that combined hardware, software, AI, and system-level integration.

Round 2: Precision PCB Design & CAD Integration Challenge

Immediately following the inauguration, round 2 of the competition began at approximately 9 a.m. Participants were presented with the challenge statement titled *"Precision Line Follower Control System – PCB Design & CAD Integration Challenge."*

Teams were required to design a compact and efficient PCB for a Line Follower Car using open-source design tools such as KiCad. The challenge demanded accurate schematic development, optimized PCB routing, proper grounding techniques, and strict adherence to predefined mechanical constraints provided through chassis reference dimensions. Participants also had to ensure reliable integration of components such as ESP32 modules, motor drivers, IR sensors, GPS modules, RFID readers, battery management systems, and power regulation circuitry.

In addition to PCB development, teams were encouraged to create a complete CAD assembly of the system for bonus evaluation. The CAD requirements included enclosure design, mounting structures, battery accessibility, ventilation, solar panel placement, connector cut-outs, and PCB integration within the mechanical assembly.

Throughout the session, mentors and organizers conducted continuous review rounds to evaluate design feasibility, routing quality, dimensional accuracy, and component integration strategies. Participants worked intensively until approximately 2:00 p.m., after which a lunch break was provided.

Following lunch, the judging panel reviewed the PCB layouts, schematics, CAD assemblies, and documentation submitted by the teams. Based on the technical evaluation and implementation quality, shortlisted teams advanced to the final round of the competition.

Round 3: Autonomous Safari Navigation System – 24 Hour Hardware Hackathon

At approximately 5:00 p.m. on 11th April 2026, the final round of Unplugged 3.0 officially commenced. This marked the beginning of the core 24-hour hardware hackathon challenge based on the problem statement titled *"Autonomous Safari Navigation System with Real-Time Tracking and Object Detection."*

Participants were tasked with designing and building a fully autonomous line-following safari vehicle capable of navigating a predefined track while simultaneously performing real-time tracking, sensor fusion, wireless communication, and object detection. The challenge required seamless integration of embedded systems, IoT communication, edge AI, computer vision, and web technologies into a single operational prototype.

The expected system capabilities included:

- Autonomous line-following navigation using IR sensors
- RFID-triggered event handling and safari completion detection
- Real-time position tracking and path visualization on a web dashboard
- Wireless telemetry transmission using IoT protocols
- Vision-based object detection and classification using onboard cameras
- Dynamic event logging and report generation
- Integration of hardware, AI models, and software interfaces into a unified autonomous workflow

Teams began intensive development immediately after the problem statement briefing. The event atmosphere reflected continuous collaboration, rapid prototyping, debugging, hardware assembly, software integration, and iterative testing.

Evening snacks were provided to participants to ensure uninterrupted workflow and maintain energy levels during the development process.

Mentor Reviews & Continuous Evaluation

During the night, multiple review and mentoring sessions were conducted to monitor progress and provide technical guidance to participants. The mentoring panel and judging panel consisted of Mr. Jay Vora, and Prof. Venkatraman.

The mentors evaluated teams on innovation, hardware implementation, PCB integration, embedded system design, AI optimization, system synchronization, and overall project feasibility. Constructive feedback provided during these reviews helped participants refine their solutions and improve system performance before final demonstrations.

Dinner arrangements were made for all participants later in the evening, followed by midnight snacks to support teams working continuously through the night. The event maintained a highly energetic and collaborative environment as teams continued coding, assembling hardware, calibrating sensors, training models, and debugging communication systems.

Overnight Development & Track Testing

As the hackathon progressed into the early hours of Sunday, participants continued refining and optimizing their systems with minimal downtime.

By early morning on 12th April 2026, teams were granted access to the official testing arena and line-following track. This testing phase was critical for validating real-world performance and ensuring reliable autonomous operation under competition conditions. Teams utilized this opportunity to:

- Fine-tune IR sensor calibration
- Optimize motor control algorithms
- Improve line-following accuracy
- Test RFID-triggered events
- Validate telemetry communication
- Evaluate object detection performance
- Synchronize onboard systems and dashboard visualization

Breakfast was provided to participants during the morning session, followed by additional mentor evaluations and technical reviews. Teams continued implementing improvements based on testing observations and reviewer feedback.

Final Demonstrations & Evaluation

Following further development and optimization, lunch was served to all participants before the commencement of the final judging session.

The final evaluation involved live demonstrations of the autonomous safari systems on the designated track. Teams showcased their fully integrated prototypes, highlighting autonomous navigation, object detection, live tracking dashboards, RFID checkpoint handling, and event logging mechanisms.

Projects were evaluated on multiple criteria, including:

- Reliability and stability of autonomous navigation
- PCB and hardware integration quality
- Embedded system performance
- AI model efficiency and object detection accuracy
- Real-time communication and dashboard responsiveness
- Innovation and scalability of the solution
- Overall system integration and presentation quality

The final judging round concluded during the evening, after which participants assembled in the Seminar Hall for the closing ceremony.

Closing Ceremony & Prize Distribution

The official closing ceremony of Unplugged 3.0 was held at approximately 6:00 p.m. on 12th April 2026 in the Seminar Hall. Faculty members, mentors, organizers, and participants gathered to celebrate the successful completion of the 24-hour hardware hackathon.

The organizing team acknowledged the dedication, technical excellence, creativity, and perseverance demonstrated by all participating teams throughout the event. Winners were announced across various categories, followed by the prize distribution ceremony.

The event concluded on a highly successful note, showcasing the participants' ability to integrate

electronics, embedded systems, AI, IoT, and mechanical design into innovative real-world engineering solutions under intense time constraints.

RESULTS & WINNING TEAMS

The competition demanded precision, resilience, and innovation. The teams that demonstrated exceptional performance were:

1st Place – PIXELMINDS
2nd Place – Solder and Forget
3rd Place – Friendly State Machines and Visionaries

EVENT PICTURES

ACKNOWLEDGEMENTS

The successful execution of Unplugged 3.0 was made possible through the coordinated efforts of the faculty and organizing team of the Department of Electronics and Telecommunication Engineering.

We extend our sincere gratitude to **Dr. Anuja A. Odhekar**, Faculty In-Charge of IETE-ISF, and **Dr. Poonam Kadam**, Faculty In-Charge of DJS Microminds, for their continuous guidance and support throughout the planning and execution of the event.

We also acknowledge **Dr. Amit A. Deshmukh**, Professor and Head of the Department, for his encouragement and for providing the platform to host such a technically enriching initiative. We acknowledge **Prof. Tanaji Biradar, Prof. Yukti Bandi, Dr. Supriya Dicholkar, Prof. Abhilasha Raghatate and Prof. Dipti Kale** for their guidance and support.

We further thank **DJS Microminds** and the **DJSCE IETE Students' Forum** for their collaboration, dedication, and seamless coordination, which ensured the smooth execution of the hackathon.

IMPACT

Unplugged 3.0 provided participants with a rigorous, real-world engineering environment that demanded both technical precision and resilience. By integrating PCB design, 3D modelling, and autonomous systems within the context of wildlife conservation, the hackathon encouraged students to think beyond isolated components and toward complete, functional systems.

The experience not only strengthened practical engineering skills but also highlighted the role of technology in addressing environmental challenges, leaving participants with a deeper appreciation for both innovation and responsibility.

The theme of wildlife conservation added a meaningful dimension to the technical challenges, encouraging participants to approach engineering with a sense of responsibility and real-world awareness.

Overall, the event successfully bridged academic learning with practical application, leaving participants with enhanced technical confidence and a deeper understanding of how engineering can contribute to sustainable solutions.

4.9 DJS Spark

- Date- 18th April 2026
- Venue- EXTC Laboratories (RF, SPL, EDL, PL, ESL, BCEL Labs) DJSCE.
- Time- 09:00 am- 01:00 pm

OBJECTIVE:

- To bridge the gap between theoretical and practical knowledge.
- To upskill and equip students with technical paper writing and research abilities.

CONTENT:

The Department of Electronics and Telecommunication Engineering (EXTC), in association with the DJSCE IETE Students' Forum (IETE-SF), organized the **Inter-College Project Competition – DJS Spark 2026** on **18 April 2026** in the **EXTC Laboratories (RF, SPL, EDL, PL, ESL, and BCEL Labs), DJSCE**, from **9:00 AM to 1:00 PM**. The competition was organized with the objective of bridging the gap between theoretical learning and practical implementation by providing a platform for students to showcase innovative technical projects, enhance their problem-solving abilities, and promote research and innovation.

The event witnessed enthusiastic participation from undergraduate engineering students representing various colleges. Students presented projects across multiple domains of Electronics, Telecommunication, Embedded Systems, Artificial Intelligence, Internet of Things (IoT), Robotics, and other emerging technologies. The competition provided an excellent opportunity for participants to demonstrate their technical knowledge, creativity, and practical implementation skills.

The event commenced with a brief inaugural session, where the participants were welcomed by the faculty members and organizing committee. The students were then guided to their respective laboratories, where project demonstrations and evaluations were conducted. An expert panel of judges visited each laboratory and evaluated the projects based on innovation, technical content, practical applicability, presentation, and overall implementation.

Each participating team presented its project, explained the design methodology, demonstrated the working model, and responded to questions from the judges. The interactive evaluation process enabled participants to receive valuable feedback and suggestions for further improvement while enhancing their presentation and communication skills.

Following the evaluation, the judges carefully assessed all the projects and selected the best entries based on predefined evaluation criteria. The winners were recognized for their innovative ideas, technical excellence, and effective project execution during the prize distribution ceremony.

The competition concluded with a vote of thanks, appreciating the efforts of the participants, judges, faculty coordinators, and student volunteers for making the event a success. Overall, **DJS Spark 2026** provided a valuable platform for students to transform theoretical concepts into practical engineering solutions, encouraging innovation, teamwork, research, and industry-oriented learning while fostering healthy competition among aspiring engineers.

Event Pictures:

Dr. Anuja Odhekar
DJ Spark Co-ordinator

Prof Amit A. Deshmukh
Prof & Head EXTC department

4.10Board of Studies meeting

- Date- 5th June 2026
- Venue- EXTC RF Laboratory,5th floor, DJSCE.
- Time- 03:00 pm- 05:00 pm

Minutes of the 12th Board of Studies meeting held on 5th June, 2026

The Board of Studies (BoS) meeting of the Department of Electronics and Telecommunication Engineering was conducted in a hybrid mode on Friday, 5th June 2026, at 3:00 p.m. onwards in the conference room at DJSCE.

The meeting was held to discuss and approve:

1. Approval of the minutes of the 11th BoS meeting.
2. Modified F. Y. B. Tech scheme semester I and II for approval effective AY 2026-27.
3. Proposed modified SEM-I F. Y. B. Tech syllabus of Engineering chemistry, Structured Programming using C effective AY 2026 – 27.
4. Proposed modified syllabus of FE Ideation and Innovation Laboratory effective AY 2026 – 27.
5. Incorporation of Coursera courses into the curriculum.
6. Approval for the content revision in the NEP DJS23 Semester V course (ADCOM).
7. Discussion and approval of the detailed scheme and syllabus of Honor Program Semester 6 for Next Generation Networks, Robotics and Automation courses.
8. Discussion and approval of Semester VII and VIII subjects (OJT and Non-OJT scheme) along with the Honors Program under the DJS23 scheme.
9. Guidelines for On Job Training (OJT) in Semester VII/VIII.
10. Approval of the examiner panel for all examinations to be conducted from November 2026 onwards for various subjects under the DJ19, DJS22, and DJS23 schemes.
11. Approval of the examiner panel for M. Tech examinations to be conducted from November 2026 onwards under the DJS24 scheme.

The meeting was attended by Principal Dr. Hari Vasudevan, Vice-Principal Dr. Narendra Shekhokar, BOS members Dr S. Mande, Dr Jaykrisnan Nair, Prof. K. P. Ray, Dr Sunil Kumar Kopparapu and faculty members of the EXTC Department.

The following were the points discussed and the suggestions provided: --

(i) For the F.Y. B. Tech Semester I course "Engineering Chemistry for Semiconductor and Electronic Applications", the BOS members suggested that the course content be delivered with appropriate linkage to higher-semester courses related to semiconductor devices and the VLSI domain, thereby highlighting its relevance and application in advanced studies.

(ii) Dr. Sunil Kopparapu suggested replacing the Structural Programming with C course with python, citing that many students are already introduced to C during their school education. However, Dr. Jay Krishnan Nair expressed a differing view. After deliberation, the BOS resolved to retain the course in the curriculum and collect student feedback on its relevance and effectiveness after Semester I before considering any future changes.

(iii) In the subject of ADCOM, Dr. Kopparapu suggested to add experiments based on error control code.

(iv) Dr. Sunil Kumar Kopparapu suggested to add industry related applications in Industrial IoT and Industry 4.0.

(v) In the subject of Optical Fibre Communication, Dr. K P Ray suggested to include details regarding free space optical communication. He also stressed on system design calculation over a certain distance considering dispersion characteristics. He further added to add case studies aligned with the topics.

(vi) In the multi-disciplinary track subject Natural Language Processing, Dr. Sunil Kumar Kopparapu members suggested to include Indian script related applications.

(vii) Dr. Mande suggested to include the book VLSI Design Flow by Sneh Saurabh as a text book for the course VLSI Physical Design in semester VIII VLSI Design Honors program.

The meeting was concluded with vote of thanks to all the members present in the meeting.

Meeting Recording Link:

Recap: https://teams.microsoft.com/meet/44748121605864?p=4wl3KW7GdX8HDYM4cY

Prof. Sheeja Nair
Autonomy Coordinator,
EXTC Dept., DJSCE

Dr. Poonam Kadam
Autonomy Coordinator,
EXTC Dept., DJSCE

Prof. Amit A. Deshmukh
Professor & Head,
EXTC Dept., DJSCE

6. ACHIEVEMENTS

7.1 Faculty Publications- Conferences / Journals

Conference publication

Sr. No	First Author	Paper Details	Indexed by
1	Dr. Amit A. Deshmukh	Amit A. Deshmukh, Tanisha Gosalia, Mihir Sanghvi, Dhyey Pau, "Microstrip Antenna Array Employing Rectangular Patches For High Gain Wideband Response", Accepted for publication in Proceedings of ICICGR 2026, SSGMCE, Shegaon, Maharastra, India, IEEE Proceedings.	IEEE
2	Dr. Amit A. Deshmukh	Venkata A. P. Chavali, Devansh Bohare, Jagat Swarup, Amit A. Deshmukh,"Electromagnetically fed Gap coupled Slot-cut Equilateral Triangular Microstrip Antenna for Wide Bandwidth", Proceedings of ICICGR 2026, SSGMCE, Shegaon, Maharastra, India, IEEE Proceedings.	Springer, LNEE
3	Dr. Prasad Joshi	S. Tilak and P. Joshi, "Evaluating the Impact of Handcrafted Feature Fusion with CNN Architectures on Ultrasound Based Muscle Health Assessment," 2025 IEEE Pune Section International Conference (PuneCon), Pune, India, 2025, pp. 1-5, doi: 10.1109/PuneCon67554.2025.11379181.	IEEE
4	Dr. Prasad Joshi	S. Tilak and P. Joshi, "FPGA Based Neural Networks for Ultrasound Muscle Pathology Classification," 2025 Second International Conference on Pioneering Developments in Computer Science & Digital Technologies (IC2SDT), Delhi, India, 2025, pp. 582-587, doi: 10.1109/IC2SDT68218.2025.11383760.	IEEE
5	Dr. Supriya Dicholkar	Prajakta P,Dhanashree p, Supriya D, Ruchi C,"Smart AR Surgical Guidance Using Artificial Intelligence", 4th International Conference on Science, Technology, Engineering & Mathematics for Sustainable Development (ICSTEMSD-2026) 24th march 2026	ISTE
6	Prof. Dipti Kale	D. Kale, G. Ganjre and R. Udani, "A Proposed Real-Time FPGA System Using MFCC Features for Acoustic Anti-Poaching Monitoring," *2026 International Conference on Communication, Computing and Emerging Technologies (IC3ET)*, Vasai, India, 2026, pp. 215-220, doi: 10.1109/IC3ET64989.2026.11467226.	IEEE

Journal publication

Sr. No	First Author	Paper Details	Indexed by
1	Prof. Amit A. Deshmukh	Amit A. Deshmukh, Aneya Soneji, Ayush Jain, Dhyey Pau, "Gap-coupled Design Of U-slot Cut Square Microstrip Antenna For Wideband Circular Polarized Response In GSM Application", International Journal of Microwave and Optical Technology, Vol. 21, no. 1, pp. 49 – 57, January 2026	Scopus
2	Prof. Amit A. Deshmukh	Amit A. Deshmukh, Devika Panicker, Aarya Gaonkar Venkata A. P. Chavali, "Elliptical Shape Microstrip Antennas Loaded with Plus Shape Slot For Compact and Wideband Circular Polarized Response", AEU International Journal of Electronics and Communication, Volume 207, March 2026, 156239,(https://doi.org/10.1016/j.aeue.2026.156239,	Scopus
3	Prof. Amit A. Deshmukh	Amit A. Deshmukh, Spoorthi Shetty, Jash Furia, Nidhi Gandhi, "Circular Microstrip Antenna Loaded With Shorting Posts and Sectoral Slots For Lower Cross-Polar Radiation", Accepted for publication in Journal of Microwaves, Optoelectronics and Electromagnetic Applications. https://www.sciencedirect.com/science/article/abs/pii/S1434841126000452).	Scopus
4	Prof. Amit A. Deshmukh	Amit A. Deshmukh, Sujay Tawde, Sanjay B. Deshmukh, "Compact Designs of U-slot cut Hexagonal Microstrip Antennas Loaded with Shorting Posts For Circular Polarized Response", Progress in Electromagnetics Research C, Vol. 170, pp. 97 – 111, 2026 (https://www.jpier.org/PIERC/pier.php?paper=26032307, http://dx.doi.org/10.2528/PIERC26032307).	Scopus

7.2 Interaction of faculty with outside world

FDP/ STTP/Webinar/Workshop attended by Faculty Members:

Sr. No.	Name Of Faculty	Details of Workshop/ Webinar/STTP/FDP	Date / Year of Event
1	Dr. Satishkumar Chavan	FDP on Recent Trends in FPGA Design and Application Development organized by Godavari College of Engineering, Jalgaon	16th -21st February, 2026
2	Dr. Poonam Kadam	SEMiX workshop by IIT Bombay	30th Jan 2026
		Five day STTP on CHIPCRAFT:Digital and Analog VLSI Chip Design usig CADENCE	29th June to 3rd July 2026
3	Yukti Bandi	Attended ATAL FDP ONLINE organized by ORIENTAL COLLEGE OF MANAGEMENT, BHOPAL	12th-17th January, 2026
4	Dr. Supriya Dicholkar	Attended ISTE-approved STTP on Digital Twins: Driving Cybersecurity, Sustainability, and Innovation across Service Sectors	19th -24th January 2026
		Attended ISTE approved online STTP on Pioneering 6G Transforming Connectivity for the Future organized by St. John, Palghar	9th Feb to 13th Feb 2026
		ISTE approved STTP on Data to Decisions	22nd June to 30th June 2026

Other Events:

Name of Faculty	Event description	Date
Prof. Amit Deshmukh	Served as external examiner for PhD APS at KJSCE, Vidyavihar.	29th June 2026
	Worked as external auditor at RGIT for external audit of EXTC department.	29th May 2026
	Served as reviewer for journals like, International Journal of Communication Systems, Progress in Electromagnetics Research, Electromagnetics, AEU.	22nd February 2026
Dr. Prasad Joshi	Session Chair – ICCCDS 2026 MULTICON-W 2026,	13th March 2026
	Reviewer at - IC3ET 2026,	9th 10th , February 2026
Dr. Ponnam Kadam	Acted as Peer reviewer for International Journal of Communication Systems., Recognized as a PEER reviewer for the international journal of Electronics.	Jan to June 2026
	Worked as resource person for full day hands on workshop on VLSI and FPGA Design organized by DJS Microminds	22nd February 2026
Dr. Vishakha Kelkar	Question paper Auditor at SPCE.	26th August 2025

	Active SPOC for NPTEL Local chapter : Swayam NPTEL	20th Jan 2026
	Member of PAQIC and Advisory committee at Thakur College of Engineering	19th Sept 2025 and 30th May 2026
Dr. Anuja A Odhekar	reviewer for 2026 International Conference on Communication, Computing and Emerging Technologies (IC3ET).	Jan 2026
Dr. Aarti G. Ambekar	Recognition as peer reviewer for the following International Journals and conferences: - IEEE ACCESS, PIER and International Journal of RF and Microwave Computer aided Engineering, International journal of Communication System by Wiley. IEEE conference ICECET'26, Rome. Italy, IEEE International Conference on Artificial Intelligence, Computer, Data Sciences and Applications (ACDSA 2026), Philippines.	Jan to June 2026
Yukti Bandi	Recognised as a PEER reviewer for the journal "Information sciences" by Elsevier	April 2026
Archana Chaudhari	Worked as Session Chair at Atharva College of Engineering	24th March 2026
Dr. Supriya Dicholkar	Worked as reviewer for ICSTEMSD 26	Jan 2026
	worked as reviewer for International Conference on Electrical, Computer and Energy Technologies (ICECET 2026) , Italy, 6th - 9th July 2026	Feb 2026
	Acted as peer reviewer for 6th International Conference on Electrical, Computer and Energy Technologies (ICECET' 26), Italy	March 2026
	Acted as peer reviewer for 6th International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME 2026), Bali,Indonesia.	June 2026

7.3 NPTEL/COURSERA Courses completed by faculty members:

Sr.No	Name Of Faculty	Details of Workshop/ Webinar/STTP/FDP	Date / Year of Event
1	Dr. Poonam Kadam.	NPTEL 12 weeks FDP on Design and Analysis of VLSI Subsystems	Jan-April 2026 (12 weeks)
		NPTEL 12week course on Microprocessors and Microcontrollers	Jan-April 2026 (12 weeks)
2	Dr. Satishkumar Chavan	NPTEL 12week FDP on Deep Learning - IIT Roper.	Jan-April 2026 (12 weeks)
3	Dr. Darshana Sankhe	NPTEL 4week FDP on Outcome based Pedagogic Principles for Effective Teaching - IIT Madras	Feb-March 2026 (4 weeks)
4	Yukti Bandi	NPTEL FDP on Machine learning	July to November 2025 (12week)
5	Bahar Soparkar	Courseera Course on Learn to teach Java: Bollean Expressions, If statements and Iteration	9th June 2026
		Courseera course on Introduction to AI Beginners	15th June 2026
6	Abhilasha Raghtate	NPTEL FDP course on "Research and Publication Ethics" with 90%	July to November 2025 (12week)
		NPTEL FDP course on "Data Analytics with Python"	Jan-April 2026 (12 weeks)
7	Dr. Supriya Dicholkar	NPTEL 12week FDP on Blockchain and it's Application	Jan-April 2026 (12 weeks)

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Prof. Vignesh Muthuvijayan
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7.4 Faculty Achievements

Name of Faculty	Event description	Date
Dr. Aarti G. Ambekar	International editorial recognition by SPRINGER NATURE as an Editorial Board member of Journal Scientific Reports for the year 2026, with following awards ' Editor of Distinction Awards 2026' namely:- Authors Service and Editorial Contribution award	May 2026
	Selected as a 2025 IEEE Access Exceptional Reviewer.	Jan 2026

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आवेदन सं. / Application No.: LD-53587/2025-CO दाखिल करने की तिथि/ Date of Filing: 22/12/2025

एतद्द्वारा यह प्रमाणित किया जाता है कि प्रतिलिप्याधिकार अधिनियम, 1957 के प्रावधानों के अनुसार, उपर्युक्त आवेदन में प्रकट किए गए "Refreshable braille actuator system for visually challenged person" नामक कार्य के लिए प्रतिलिप्याधिकार प्रदान किया गया है।

This is to certify that a copyright has been registered for the work titled "Refreshable braille actuator system for visually challenged person" as disclosed in the below mentioned application in accordance with the provisions of the Copyright Act,1957.

रचयिता / Authors:

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4	AMIT A. DESHMUKH	NO. U-15, BHAKTIVEDANTA SWAMI RD, OPP. COOPER HOSPITAL, NAVPADA, VILE PARLE WEST, MUMBAI-400056

स्वामी / Owners:

सं. / SNO.	नाम / Name	पता / Address
1	SVKM'S DWARKADAS J. SANGHVI COLLEGE OF ENGINEERING	NO. U-15, BHAKTIVEDANTA SWAMI RD, OPP. COOPER HOSPITAL, NAVPADA, VILE PARLE WEST, MUMBAI-400056

प्रकाशक विवरण / Publisher Details: N.A.

कार्य की भाषा / Language of the Work: English

कार्य का विवरण / Description of the Work: An assistive system with ESP 32 camera is proposed for visually challenged person that translates printed text into tactile braille patterns for display on a refreshable braille actuator system.

(शर्तें / टिप्पणियाँ, यदि कोई हो) / (Conditions/ Remarks, if any): N.A.

आर. ओ. सी. जारी होने की तिथि / Date of ROC: 29/06/2026

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For Additional details please see next page.

Page 1 of 2

Prof. Supriya Dicholkar successfully defended PhD on **25th August 2025**
Topic name: **Modelling Framework for Detections of Attacks in IoT Network**
Name of University: **Mumbai University**

Prof. Chandrashekhar Beral successfully defended PhD on 4th June 2026
Topic name: **Priority Based Congestion Controlling Mechanism for Wireless Sensor Network to Healthcare System**
Name of University: **Sant Gadge Baba Amravati University**

7.5 Student's participation in various events

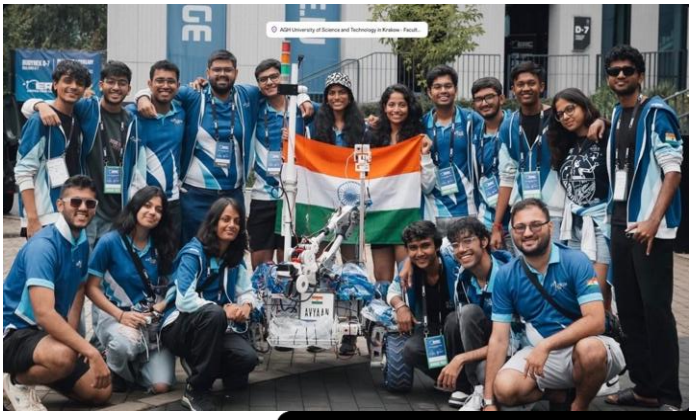
Sr. No.	Student Name	Type of Event	Date	Award/ Achievement
1	Arnav Bhandari	National Project Competition at Nscif (Delhi),Tatva enviropreneure,Iit Codeversity ,Startup Showdown,Kjsce Agritech Hackathon ,Djs Strike Connecting dreams foundation(Nscif),Tatva(Iit Bombay),Codeversity(Iit gandhingar),Finance Club(iit Patna),Ecesa(Kjsce respectively	Jan to June 2026	30000,75000,35000
2	Trushna Hadawale	National Project Competition at Oscillations 3.0 , Technovate (Dy Patil), Prakalp (Kj somaiya), PRAKALP 4.0 (Fr Agnel) at Thakur College of Engineering, DY patil college, KJ somaiya college of engineering, Fr Agnel Institute of technology	Jan to June 2026	1st prize in Technovate , 2nd prize in oscillation 3.0 , 3rd prize in Prakalp, 1st runner up in PRAKALP 4.0.
3	Heet Bharadwa	National Project Competition at 1st at Iit Gandhinagar codevercity hackathon, 1st at IIT Bombay tatva enviropreneur sustainability, 1st runner up at AGRITECH a national level hackathon at kjsce, 1st runner up at djs spark, 1st runner up at DJS strike, 2nd runner up at velora 1.0 at mitaoe pune.	Jan to June 2026	1st position at Iit Gandhinagar codevercity hackathon, 1st position at IIT Bombay tatva enviropreneur sustainability, 1st position runner up at AGRITECH a national level hackathon at kjsce, 1st runner up at djs spark, 1st runner up at DJS strike, 2nd runner up at velora 1.0 at mitaoe pune
4		Course completed of Make your own board on Udemy, pcb designing on altium, Arduino for all by edouard renard, complete digital marketing guide 27in 1 by Robin and jesper, Ltspicevtutorial by yezhao, phd, my equation's robo ai.by Udemy and Myequation	Jan to June 2026	Completed
5	Mishti Damania	National level project competition Prodnosis(Technex'26) by IIT BHU(Varanasi)	13th -15th march 2026	First position with prize amount of 50,000
6	Varun Nitin Mutha	National level project competition of Hackanova 5.0, DJS STRIKE 2026 organized by Thakur College of Engineering and Technology, Dwarkadas J. Sanghvi College of Engineering	16th March 2026	Won First Prize of 20000
7	Yash Patil	Redbull wings for life run organized by Kj Somaiya college	10th May 2026	8.5 km running medal
8	Dhrish Jain	Completed Embedded system Internship	18th	6 months Internship

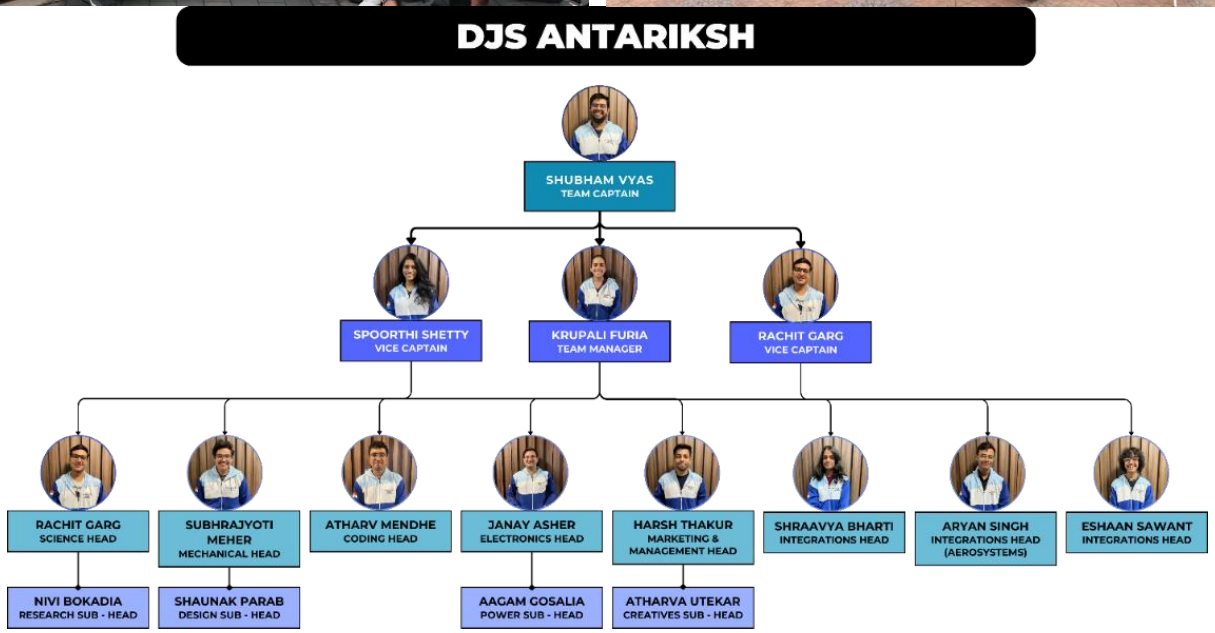
		at Aican pvt ltd	October 2025 to 18th April 2026	
9	Agrim Tawani	International Project Competition Yellow Hackathon 2026 at IIT delhi prganised by Bizthon - Global Hackathon Organiser Company		Won 1st Prize 5,000 USD -
7	Urva Jitendra Gala	Project Competition in DJS Spark	18th April 2026	5th rank in dj spark
8	Nilay Mistry	Project Competition in Dj spark, tech expo, dj strike	18th April 2026	3rd in dj spark
9	Tanush dhiraj maloo	National and International Project Competition at Hack4safety, Sih, autonomous hacks 2026, hackthetank3.0, khacks3.0,l oc8.0, techathon, hultxIIC, hackanova, strike, spark organized by Ministry of coal, government of India and multiple student chapters	Dec to May 2026	winner
10	Tanay Kamdar	Workshop at Speedsters Competition organized by FMAE Project Competition;	7th October 2025	10 days' workshop completed
11	Parth Dani	12 hr ICC Cricket Sports; Super striker season cricket tournament held at N L Ground Dahisar	15th April 2026	Player of the match and runner up medal
12	Vyapti Shah	1week Workshop on build with India Hackathon organized by Google	April 2026	Completed
13	Varun Nitin Mutha	National level Project Competition Hackanova 5.0, DJS STRIKE 2026 held at Thakur College of Engineering and Technology, DJSCE IETE - ISF	16th March 2026	Won prize of 20,000
14	Vinay Sanjaykumar Karawadiya	National level Project Competition at DJSCE	16th March 2026	Won top position
15	Karan Shah	National level Project Competition Unplugged, strike, spark	March, April 2026	unplugged-participate, tech expo - participant, strike - winner, spark - 3rd
16		DJS TRINITY SPORTS Cricket, Basketball At DJSCE	12th March 2026	Cricket -winner basketball-runners up
17	Krish tawde	Cultural; DJS Trinity Fashion Show	16th March 2026	1st place
18		4hr PLC workshop	14th February 2026	Completed
19		National level Project Competition; Djs Strike, Djs Spark	March April 2026	4th and 3rd place respectively
20	Varun Vaidya	National level Project Competition; Tech-a-thon at Thadomal shahani engineering college by Electraverse	March 2026	Selected in Top 30 position

		committee		
21	Manish Yadav	Striders 2 Hr National level Marathon at Thane	8th Feb 2026	Completed under time
22		National level Project Competition organized by ArtPark IISc Bangalore on the topic Ground station for SmartKrishi system	17th July 2025	Participated
23		Course completed on 28hour Udemy ROS2 Moveit2	20th April 2026	Completed
24	Anees Alwani	2 months Internship completed at Eyantra IIT-Bombay	19th May to 11th July 2025	Completed
25	Suman Swain	I9 months Internship at Pixiq Cinetech	11th June 2025 to 31st March 2026	Completed
26		AI Agents Workshop organized by Reliance Foundation	14th April 2026	Completed
27	Mayuresh Thakur	Internship by Deepcytes Cyberlabs	2nd June 2025 to 14th December 2025	Completed
28	Aagam Gosalia	SVKM YUVA FEST 3 days cricket organized by NMIMS Shirpur	12th to 14th Jan 2026	Runners up in cricket
29		Presented paper Iot based health monitoring system at International conference ICTEAH organized by K J Somaiya	16th April 2026	Published paper
30	Atharva Sunil Wadekar	The project competition was aimed to make a high-speed drone for drone race competition organized by DJS Trinity	March 2026	Second runner up certificate
31	Aangi Gada	6 months course completed on Microsoft Data Visualization and Power BI - Courseera 2. Python in Data Science by IBM - Coursera	4th Jan 2026	Completed
32	Tanushka Waghela	Participated in Trinity IDPT Volleyball and Cricket organized by DJSCE	16th and 20th Feb 2026	Won in Cricket
33		Svkm Yuva Sports Volleyball Competition, Enertia Volleyball Tournament organized by Svkm' Mrp School Tande, Thakur College of Engineering respectively	12th and 13th Jan 2026 and 12th March 2026	Winners , Runner's Up respectively
34	Vatsal Maru	Internship at Wipro	Jan to June 2026	Completed

DJS Antariksh Team Introduction

DJS Antariksh is the official Martian Rover Team of Dwarkadas J. Sanghvi College of Engineering, Mumbai, affiliated with Mumbai University. Founded in 2019, the team operates under the motto **"To Decipher Unimaginable,"** reflecting its commitment to pushing the frontiers of space exploration through innovation. The team consists of 60 passionate second- and third-year undergraduate students from various engineering backgrounds, organized into five key departments: **Mechanical, Electronics, Coding, Science, as well as Marketing and Management.**





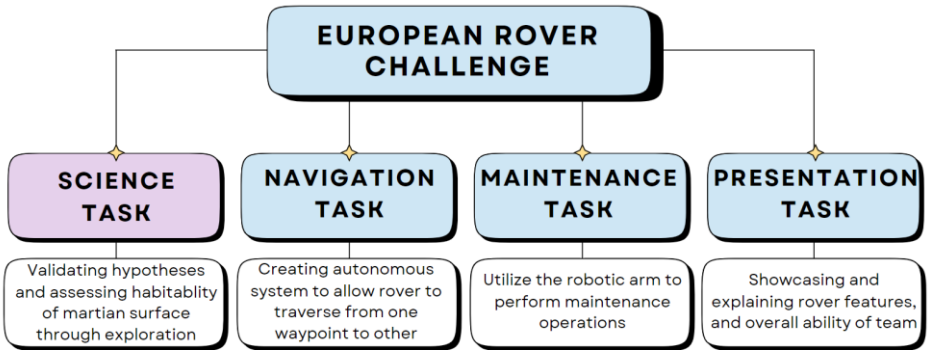
Competitions

3. European Rover Challenge

European Rover Challenge

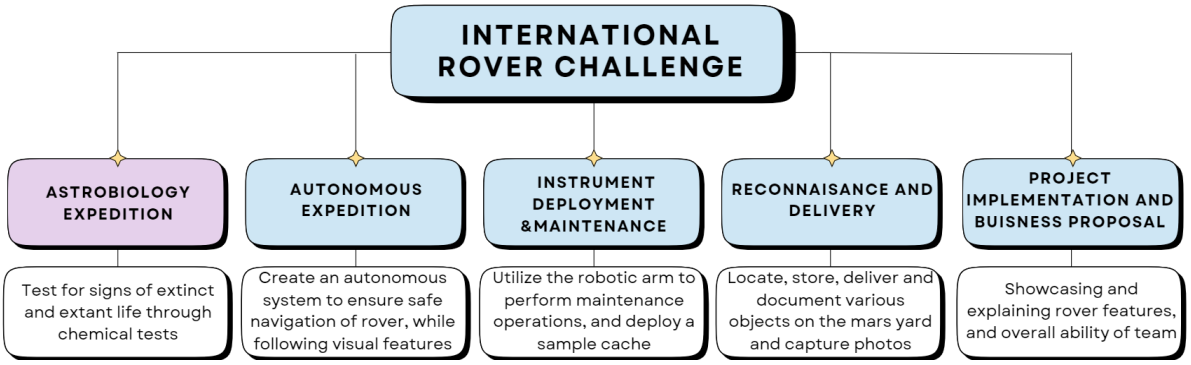
The European Rover Challenge organized by the European Space Foundation takes place every year in Poland. It is an integrated programme working towards technological developments, specifically those in GPS-denied environments, with space exploration and utilization as the leading

theme. The ultimate goal of the ERC is to become a standardized test trial and benchmark for planetary robotic activities, coupled with strong professional career development platform.. The event brings together university teams to design and operate Martian rover prototypes that are tested on a Mars-like terrain. The competition includes tasks such as autonomous navigation, astrobiology tasks, maintenance operations giving teams a practical platform to apply and test their engineering work. Over the years, the team's participation at ERC has helped steadily improve rover designs, strengthen technical approach, and build consistency in performance on the international stage. Through these achievements, the team has also been able to represent the college and bring recognition to it at a global level.



4. International Rover Challenge

The International Rover Challenge is an international competition organised by the Space Robotics Society. It challenges university students to conceptualise, design, develop and operate an astronaut-assistive next-generation space Rover. The objective of the competition is to provide students with a real-world interdisciplinary engineering experience, combining practical engineering skills with soft skills, including business planning and project management.



ERC On-site Qualification:

In the ERC 2025 Qualification Round**,** DJS Antariksh secured 1st place worldwide, finishing at the top among 102 participating teams from multiple countries across the globe. This achievement qualified DJS Antariksh for the On-Site Finals in Poland**,** marking a proud moment for the team.

ERC 2025 Result

At the ERC 2025 On-Site Finals in Poland, DJS Antariksh secured 7th place worldwide**,** 1st in Asia and 1st in India reflecting steady growth and consistent performance in the competition over the years.

1		DJS ANTARIKSH	234.5 pts	13		WARRYZN Space Robotics	212.2 pts
2		EPFL Xplore	230.7 pts	14		Team Raptors PL	212.1 pts
3		4Space	226.9 pts	15		ProjectRED	211.7 pts
4		STAR Dresden e.V.	225.8 pts	16		SKA Robotics	210.5 pts
5		ASU ROAR	223.9 pts	17		KNR Rover Team	210 pts
6		Beyond Robotics	218.5 pts	18		OzU Rover Team	207.5 pts
7		DIANA	218.5 pts	19		AAU Space Robotics	207.3 pts

No.	Team's Name	Country	ERC FINAL SCORE (max 3000 pts)
1	EPFL Xplore	Switzerland	2180,4
2	STAR Dresden e.V.	Germany	2147,84
3	AGH Space Systems	Poland	2048,05
4	DIANA	Italy	1927,94
5	FHNW Rover Team	Switzerland	1801,9
6	Team Raptors PL	Poland	1770,3
7	DJS Antariksh	India	1743,5
8	SKA Robotics	Poland	1622,7
9	KNR Rover Team	Poland	1554,9
10	Mars Rover Manipal	India	1530,2

Cansat Competition 2026

Team DJS Arya - Dwarkadas J. Sanghvi College of Engineering

This document serves as the official record of the achievements secured by **Team DJS ARYA, DJ Sanghvi College** at the **International CanSat Competition 2026**. Following the conclusion of the final evaluation phases and the release of the official standings, the team has achieved historic **milestones on both institutional and international levels.**

About the Competition

The Cansat Competition is organized every year by **American Astronautical Society** in collaboration with **NASA** at **Virginia, USA.** The annual International CanSat competition challenges university teams to design and build a complex, **two-part simulated satellite system** consisting of a container and a sensor-driven payload.

For the 2026 mission, the rocket deploys the system at peak altitude, where it initially descends under a primary parachute before the payload separates at 80% altitude. Once separated, the payload must **autonomously steer toward a designated target coordinate using a custom-engineered paraglider descent control system**, all while recording dual-camera video and 1 Hz sensor telemetry - including GPS, tilt angle, and battery metrics - back to a custom ground station. Just two meters before hitting the ground, the payload is required to safely release its onboard scientific **instrument - simulated by a fragile hen's egg - ensuring it lands entirely intact.**

1. The Mark Walker Best Ground Station Award 2026

DJS ARYA was officially awarded the prestigious Mark Walker Best Ground Station Award. The award was established in memory of Mark Walker, a brilliant engineer who spent his career instructing teams globally.

This honour is presented to the team demonstrating the Innovative Ground Station Design for its uniqueness and ability to stand out. The Ground station was judged on parameters like ease of Access, Usability, Performance and reliability. The whole ground station was designed from Scratch, the team made the Enclosure, the custom keycap Keyboard and Software for the GUI - all in house.

HIGHLIGHTS:

- **Number 1 in the World:** We walked away with the **Mark Walker Best Ground Station Award**, officially taking the **#1 spot globally** for our ground station. Marking DJS Arya's Spot as amongst the best teams globally.

- **The Pokémon Vision:** Instead of building another boring, sterile gray box, we took a massive creative risk and designed the entire station around a nostalgic **"Pokedex"** theme. We wanted it to feel like a high-tech field terminal analysing the Flight of the Cansat In real time with hints of Pokemon bits spread all across.

- **Enclosure, Laptop-Free Build:** We engineered a custom, standalone field enclosure completely from scratch. Build to perfectly enclose the Screen, Electronic components necessary to run the GCS, and all the required RF modules. We didn't go for pre-made laptop components and combined parts like RaspberryPi, Screen and Input devices Etc. Our custom-made Keyboard with Each key being painted by hand in Pokemon theme made it stand out the most.

- **A Gamified GUI:** We completely customized the user interface to match the vibe. It used a Linux Shell distribution which ran our custom software. The Different Status Icons and labels were made to match the Pokemon theme, with various animations making the UI feel nostalgic and different. Yet managing to fully showcase all necessary flight parameters of the cansat.

2. Global and Regional Standings

The team's cumulative score across the Preliminary Design Review (PDR), Critical Design Review (CDR), and Launch Operations secured elite ranks across national, continental, and global leaderboards:

ALL INDIA RANK (AIR): 1ST
ASIA RANK: 4TH

WORLD RANK: 10TH

Team	Country	FINAL
1043	Thailand	93.0778%
1093	United States	92.7877%
1064	Indonesia	91.5926%
1094	United States	90.2816%
1081	Argentina	86.1917%
1059	Thailand	84.5877%
1088	Italy	84.0266%
1001	Canada	82.9035%
1009	México	81.7846%
1038	India	81.2150%
1083	United States	81.1971%
1002	Argentina	80.8082%
1110	United States	80.6180%
1049	Germany	78.1757%
1082	Turkiye	75.5596%
1091	Poland	75.0926%
1092	Poland	74.9765%
1070	Republic of Korea	74.6013%
1006	India	74.2434%
1127	Türkiye	72.4974%
1096	United States	71.9131%
1073	Mexico	71.1889%
1035	Singapore	70.8401%
1007	Colombia	70.6597%
1011	Canada	70.0134%
1075	United States of America	69.7555%
1003	Uzbekistan	68.8341%
1114	Italy	67.8023%
1041	Hong Kong SAR	64.6237%
1079	United Kingdom	64.0939%
1062	South Korea	61.4967%
1015	United States	57.0072%

This year's results aren't just a win, they are the **absolute highest scores and the single best performance** DJS ARYA has ever put up. By locking in **All India Rank 1**, we officially held onto our crown as the undisputed number one team in the country. But we didn't stop there. We pushed further onto the international stage than we ever have before, taking a massive **4th place in Asia** and breaking into the elite global top ten with an incredible **10th place finish in the world overall alongside the Mark Walker Award.**

Reaching a world rank this high is a massive milestone for us, and it completely cements the team as a legitimate global competitor in student aerospace challenges. We've officially set a brand new benchmark, and honestly, the bar has never been higher.

Thank you

7 RESULT ANALYSIS

Academic Year : 2025-26

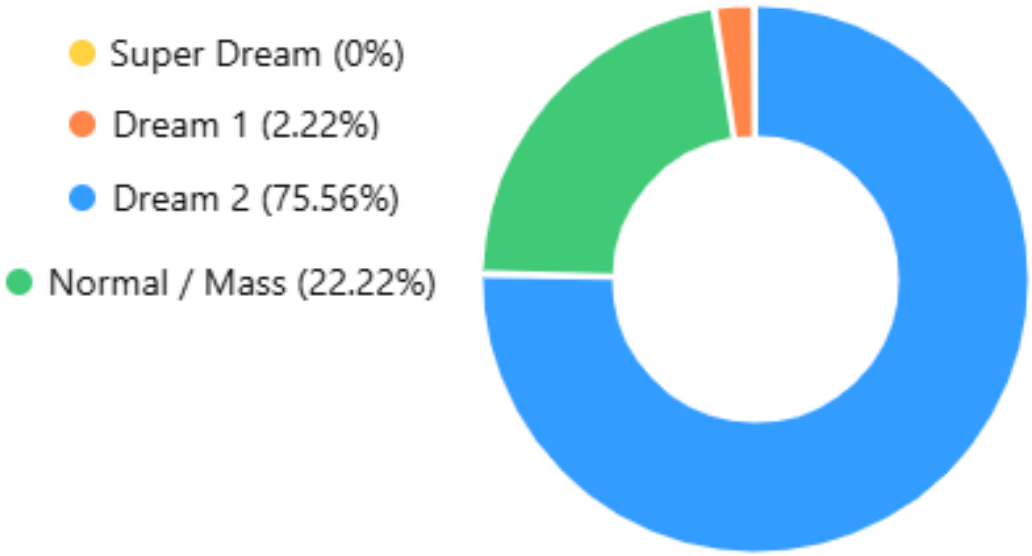
Sr. no.	Semester	Total no of students appeared	Total no of students passed	% of passing in the subject
1	III	204	191	93.63
2	V	205	191	93.17
3	VII	211	205	97.16

8 PLACEMENT DATA

Total no. of Students Placed Company Wise = 90 (Including Multiple Placement Offers)

Sr. No.	Company Name	Package (CTC in LPA)	No. of Students Placed
1	ZS (Campus Beats)	14.15	2
2	Here Technologies	12.00	1
3	Jaro Education	10.16	1
4	Sure. Financial	10.00	1
5	TCS (Digital) TCS (Prime) TCS (Ninja)	9.09 7.09 3.46	26
6	Jio World Centre	8.88	1
7	Indus Valley Partners	8.52	1
8	Quantiphi	8.50	2
9	TresVista	8.40	1
10	Articulus Surgical	8.00	1
11	Godrej Enterprises Group	7.87	2
12	Veefin	7.50	6
13	Zeus Learning	7.10	1
15	Aditya Birla Group – Ultratech	7.00	2
16	Fractal Analytics	7.00	1
17	LenDenClub	7.00	1
18	Deloitte	6.71	3
19	GEP	6.50	3
20	Frootle	6.00	4
21	KPMG	6.00	2
22	DeltaX	6.00	1
23	Squareyards	5.00	2
24	Gandhi Automation	4.60	2
25	Capgemini	4.25	19
26	Pazago	4.25	1
27	Aura Jewels	4.20	1

Minimum CTC in LPA: 3.46 LPA	Maximum CTC in LPA: 14.15 LPA



Super Dream: > 20 LPA , Dream 1: > 12 LPA and less than 20 LPA, Dream 2 : 4 LPA and less than 12 LPA, Normal / Mass : < 4 LPA